PHILIPS

Data handbook

PHILIPS

Electronic components and materials

Semiconductors and integrated circuits

Part 6 April 1974

Digital Integrated Circuits

DTL, CML, MOS

SEMICONDUCTORS AND INTEGRATED CIRCUITS

Part 6 **April 1974**

General	
DTL	FC family
CML	GX family
MOS	FD family
MOS	FE family

Index and maintenance type list at the back

Argentina
FAPESA I.y.C.
Av. Crovara 2550
Tel. 652-7438/7478
BUENOS AIRES

Australia
Philips Industries Ltd.
Elcoma Division
67-71 Mars Road
Tel. 42 1261
LANE COVE, 2066, N.S.W.

Austria
Österreichische Philips
Bauelemente Industrie G.m.b.H.
Zieglergasse 6
Tel. 93 26 22
A1072 VIENNA

Belgium
M.B.L.E
80, rue des Deux Gares
Tel. 23 00 00
1070 BRUSSELS

Brazil
IBRAPE S.A.
Av. Paulista 2073-S/Loja
Tel. 278-1111
SAO PAULO, SP.

Canada
Philips Electron Devices
116 Vanderhoof Ave.
Tel. 425-5161
TORONTO 17, Ontario

Chile
Philips Chilena S.A.
Av. Santa Maria 0760
Tel. 39-40 01
SANTIAGO

Colombia
SADAPE S.A.
Calle 19, No. 5-51
Tel. 422-175
BOGOTA D.E. 1

Denmark
Miniwatt A/S
Emdrupvej 115A
Tel. (01) 69 16 22
DK-2400 KØBENHAVN NV

Finland
Oy Philips Ab
Elcoma Division
Kaivokatu 8
Tel. 1 72 71
SF-00100 HELSINKI 10

France
R.T.C.
La Radiotechnique-Compelec
130 Avenue Ledru Rollin
Tel. 357-69-30
PARIS 1

Germany
Valvo G.m.b.H.
Valvo Haus
Burchardstrasse 19
Tel. (0411) 3296-1
2 HAMBURG 1

Greece
Philips S.A. Hellénique
Elcoma Division
52, Av. Syngrou
Tel. 915 311
ATHENS

Hong Kong
Philips Hong Kong Ltd.
Components Dept. (Kowloon Branch)
Din Wai Industrial Building, 11th Floor
49 Hoi Yuen Road, Kwun Tong
Tel. K-42 82 05-8
HONG KONG

India
INBELEC Div. of
Philips India Ltd.
Band Box House
254-D, Dr. Annie Besant Road
Tel. 457 311 to 15
Prabhadevi, BOMBAY-25-DD

Indonesia
P.T. Philips-Ralin Electronics
Elcoma Division
Djalan Gadjah Mada 18
Tel. 44 163
DJAKARTA

Ireland
Philips Electrical (Ireland) Ltd.
Newstead, Clonskeagh
Tel. 69 33 55
DUBLIN 14

Italy
Philips S.p.A.
Sezione Elcoma
Piazza IV Novembre 3
Tel. 69 94
MILANO

Japan
NIHON PHILIPS
32nd Fl., World Trade Center Bldg.
5, 3-chome, Shiba Hamamatsu-cho
Minato-ku
Tel. (435) 5204-5
TOKYO

Mexico
Electrónica S.A. de C.V.
Varsovia No. 36
Tel. 5-33-11-80
MEXICO 6, D.F.

Netherlands
Philips Nederland B.V.
Afd. Elonco
Boschdijk 525
Tel. (040) 79 33 33
EINDHOVEN

New Zealand
EDAC Ltd.
70-72 Kingsford Smith Street
Tel. 873 159
WELLINGTON

Norway
Electronica A.S.
Middelthunsgate 27
Tel. 46 39 70
OSLO 3

Peru
CADESA
Jr. Ilo, No. 216
Appartado 10132
Tel. 27 7317
LIMA

Philippines
EDAC
Philips Industrial Dev. Inc.
2246 Pasong Tamo Street
Tel. 88-94-53 (to 56)
MAKATI-RIZAL

Portugal
Philips Portuguesa S.A.R.L.
Av. Eng. Duharte Pacheco 6
Tel. 68 31 21
LISBOA 1

Singapore
Philips Singapore Private Ltd.
8th Floor, International Building
360 Orchard Road
Tel. 37 22 11 (10 lines)
SINGAPORE-9

South Africa
EDAC (Pty.) Ltd.
South Park Lane
New Doornfontein
Tel. 24/6701-2
JOHANNESBURG

Spain
COPRESA S.A.
Balmes 22
Tel. 232 66 80
BARCELONA 7

Sweden
ELCOMA A.B.
Lidingövägen 50
Tel. 08/67 97 80
10250 STOCKHOLM 27

Switzerland
Philips A.G.
Edenstrasse 20
Tel. 01/44 22 11
CH-8027 ZUERICH

Taiwan
Philips Taiwan Ltd.
San Min Building, 3rd Fl.
57-1, Chung Shan N. Road
Section 2
P.O. Box 22978
Tel. 553101-5
TAIPEI

Turkey
Türk Philips Ticaret A.S.
EMET Department
Gümüssuyu Cad. 78-80
Tel. 45.32.50
Beyoglü, ISTANBUL

United Kingdom
Mullard Ltd.
Mullard House
Torrington Place
Tel. 01-580 6633
LONDON WC1E 7HD

United States
North American Philips
Electronic Component Corp.
230, Duffy Avenue
Tel. (516) 931-6200
HICKSVILLE, N.Y. 11802

Uruguay
Luzilectron S.A.
Rondeau 1567, piso 5
Tel. 9 43 21
MONTEVIDEO

Venezuela
C.A. Philips Venezolana
Elcoma Department
Av. Principal de los Ruices
Edif. Centro Colgate
Apartado 1167
Tel. 36.05.11
CARACAS

DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, subassemblies and materials; it is made up of three series of handbooks each comprising several parts.

ELECTRON TUBES	**BLUE**
SEMICONDUCTORS AND INTEGRATED CIRCUITS	**RED**
COMPONENTS AND MATERIALS	**GREEN**

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

ELECTRON TUBES (BLUE SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1a Transmitting tubes for communications and Tubes for r.f. heating Types PB2/500 ÷ TBW15/125 — **April 1973**

Part 1b Transmitting tubes for communication — **May 1973**
Tubes for r.f. heating
Amplifier circuit assemblies

Part 2 Microwave products — **August 1973**

Communication magnetrons
Magnetrons for micro-wave heating
Klystrons
Traveling-wave tubes
Diodes
Triodes
T-R Switches
Microwave Semiconductor devices
Isolators Circulators

Part 3 Special Quality tubes; — **March 1972**
Miscellaneous devices

Part 4 Receiving tubes — **September 1973**

Part 5a Cathode-ray tubes — **November 1973**

Part 5b Camera tubes; Image intensifier tubes — **December 1973**

Part 6 Products for nuclear technology — **January 1974**
Photodiodes

Photomultiplier tubes
Channel electron multipliers
Geiger-Mueller tubes
Neutron tubes
Photo diodes

Part 7 Gas-filled tubes — **February 1974**

Voltage stabilizing and reference tubes
Counter, selector, and indicator tubes
Trigger tubes
Switching diodes
Thyratrons
Ignitrons
Industrial rectifying tubes
High-voltage rectifying tubes

Part 8 T.V. Picture tubes — **November 1972**

SEMICONDUCTORS AND INTEGRATED CIRCUITS (RED SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1a Rectifier diodes and thyristors — **December 1972**

Rectifier diodes
Voltage regulator diodes
Transient suppressor diodes
Thyristors, diacs, triacs
Ignistors
Rectifier stacks

Part 1b Diodes — **December 1972**

Small signal germanium diodes
Small signal silicon diodes
Special diodes
Voltage regulator diodes
Voltage reference diodes
Tuner diodes

Part 2 Low frequency and deflection transistors — **January 1973**

Part 3 High frequency and switching transistors — **February 1973**

Part 4a Special semiconductors — **March 1973**

Transmitting transistors
Microwave devices
Field effect transistors
Dual transistors
Microminiature devices for thick- and thin-film circuits

Part 4b Devices for opto-electronics — **March 1973**

Photosensitive diodes and transistors
Light emitting diodes
Infra-red sensitive devices
Photocouplers
Photoconductive devices

Part 5 Linear integrated circuits — **July 1973**

Part 6 Digital integrated circuits — **April 1974**

DTL (FC family)
CML (GX family)
MOS (FD family)
MOS (FE family)

COMPONENTS AND MATERIALS (GREEN SERIES)

These series consists of the following parts, issued on the dates indicated.

Part 1 **Circuit Blocks, Input/Output Devices, Electro-mechanical Components, Peripheral Devices** — **January 197**

Circuit blocks 40-Series and CSA70
Counter modules 50-Series
Norbits 60-Series, 61-Series
Circuit blocks 90-Series
Input/output devices
Electro-mechanical components
Peripheral devices

Part 2 **Resistors, Capacitors** — **April 197**

Electrolytic capacitors
Paper capacitors and film capacitors
Ceramic capacitors
Variable capacitors
Fixed resistors
Variable resistors
Non-linear resistors (VDR, LDR, NTC, PTC)

Part 3 **Radio, Audio, Television** — **June 197**

FM tuners
Loudspeakers
Television tuners, aerial input assemblies
Components for black and white TV
Components for colour television
Deflection assemblies for camera tubes

Part 4a **Soft ferrites** — **October 197**

Ferrites for radio, audio and television
Small coils
Ferroxcube potcores and square cores
Ferroxcube transformer cores

Part 4b **Piezoelectric Ceramics, Permanent magnet materials** — **October 197**

Part 5 **Ferrite core memory products** [1] — **January 197**

Ferroxcube memory cores
Matrix planes and stacks
Core memory systems

Part 6 **Electric Motors and Accessories** — **March 197**

Small synchronous motors
Stepper motors
Miniature direct current motors

Part 7 **Circuit Blocks** — **September 197**

Circuit blocks 100 kHz -Series
Circuit blocks-1-Series
Circuit blocks 10-Series
Circuit blocks for ferrite core memory drive

---

[1]) 4 Chapters of our former Part 5 (August 1972) are no longer included : chapter "Magnetic heads" has been withdrawn, chapters "Quartz crystal units" and "Variable mains transformers" are published as separate booklets, chapter "Microwave devices" has been transferred to the blue Handbook Series "Electron tubes" Part 2.

General

Preface

Type designation

Package outlines

Handling MOS devices

Graphical symbols

Ratings

Letter symbols

PREFACE TO DATA OF INTEGRATED CIRCUITS

1. General

The published data comprise particulars needed by designers of equipment in which integrated circuits are to be incorporated, and criteria on which to base acceptance testing of such circuits. For ease of reference, the data on each circuit are grouped according to the several headings discussed below.
The limiting values quoted under the headings Characteristics and Package Outline may be taken as references for acceptance testing.
Values cited as typical are given for information only.
For an explanation of the type designation code, see the section Type Designation.
For an explanation of the letter symbols used in designating terminals and performance of integrated circuits, and the electrical and logic quantities pertaining to them, see the section Letter Symbols.

2. Quick Reference Data

The main properties of the integrated circuit summarized for quick reference

3. Ratings

Ratings are limits beyond which the serviceability of the integrated circuit may be impaired. The ratings given here are in accordance with the Absolute Maximum System as defined in publication no. 134 of the International Electrical Commission; for further details see item 2 of the section Rating Systems.
If a circuit is used under the conditions set forth in the sections Characteristics and Additional System Design Data, its operation within the ratings is ensured.

4. Circuit diagram

Circuit diagrams and logic symbols are given to illustrate the circuit function. The diagrams show only essential elements, parasitic elements due to the method of manufacture normally being omitted. The manufacturer reserves the right to make minor changes to improve manufacturability.

5. System Design Data and Additional System Design Data

System Design Data normally derived from the Characteristics and based on worst-case assumptions as to temperature, loading and supply voltage, are quoted for the guidance of equipment designers. Supplementary information derived from measurements on large production samples may be given under Additional System Design Data.

6. Application information

Under this heading, practical circuit connections and the resulting performance are described. Care has been taken to ensure the accuracy and completeness of the information given, but no liability therefor is assumed, nor is licence under any patent implied.

7. Characteristics

Characteristics are measurable properties of the integrated circuit described. Under a specific set of test conditions compliance with limit values given under this heading establishes the specified performance of the circuit; this can be used as a criterion for acceptance testing.
Values cited as typical are given for information only and are not subject to any form of guarantee.

8. Logic symbols (digital circuits)

Graphical logic symbols accord with MIL standard 806B.
Supplementary drawings correlate logic functions with pin locations as a help to laying out printed circuit boards.

9. Outline drawing and pin 1 identification

Dimensional drawings indicate the pin numbering of circuit packages.
Dual in-line packages have a notch at one end to identify pin 1.
Take care not to mistake adventitious moulding marks for the pin 1 identification.
Flat packs identify pin 1 by a small projection on the pin itself and/or by a dot on the body of the package.
Metal can encapsulations identify pin 1 by a tab on the rim of the can.

PRO ELECTRON TYPE DESIGNATION CODE

The type number consists of three letters followed by a four digit serial number (sometimes augmented by a version letter).

First two letters:

Family circuits

The first two letters identify the family.

Solitary circuits

The first letter identifies the circuit as:

S-digital
T-analogue
U-mixed analogue/digital

The second letter has no special significance.

The third letter indicates the operating ambient temperature range or another significant characteristic. Letters B to F stand for the following temperature ranges: [1])

B: 0 to +70 °C
C: −55 to +125 °C
D: −25 to +70 °C
E: −25 to +85 °C
F: −40 to +85 °C

When no temperature range is specified, the third letter is A. Other third letters identify special family versions or treatments (e.g. radiation hardened).

The serial number following the three letters may be either a 4-digit number or a proprietary type designation comprising a combination of letters and digits. Proprietary type designations consisting of less than 4 characters are extended to 4 by putting zeros (0) before them.

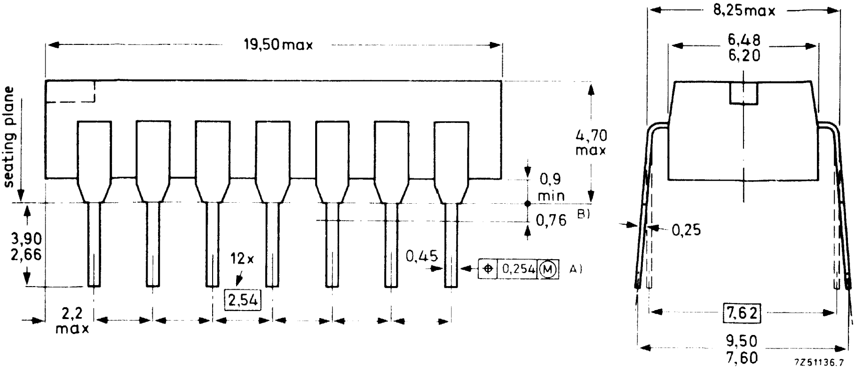
---

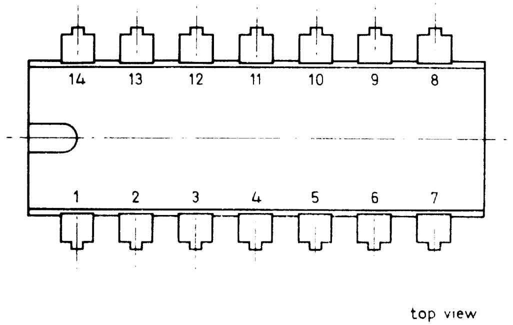
[1]) If a circuit is published for a wider temperature range, but does not qualify for another classification, the letter designating the nearest narrower temperature range is used.

Package outlines

14 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm





A) Centre-lines of all leads are within ± 0,127 mm of the nominal positons shown: in the worst case, the spacing between any two leads may, deviate from nominal by ±0,254 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

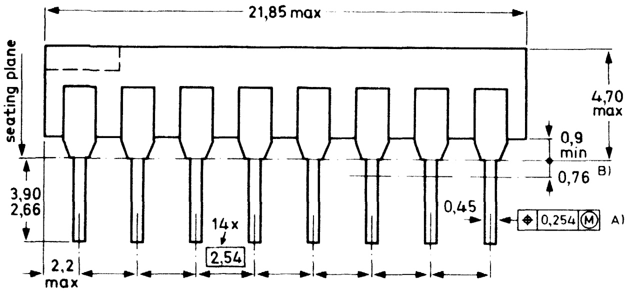
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

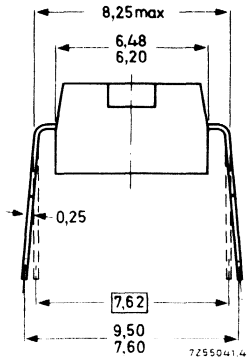
3. Repairing soldered joints

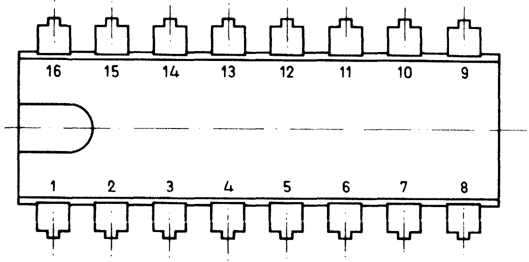
   The same precautions and limits apply as in (1) above.

16 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm







top view

A) Centre-lines of all leads are within ±0, 127 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0, 254 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

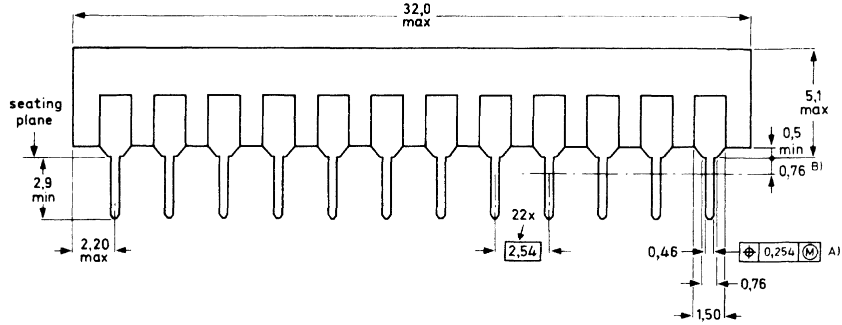
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

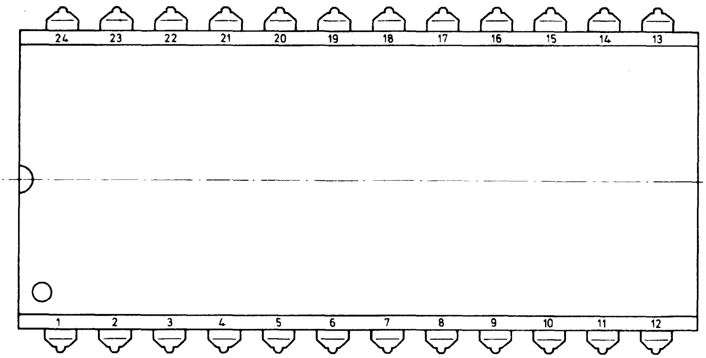
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

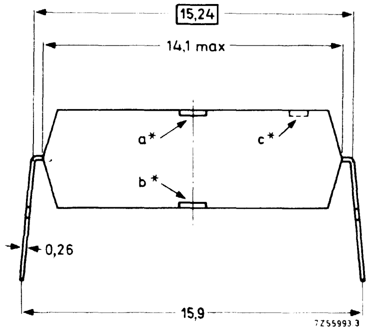
24 LEAD PLASTIC DUAL IN-LINE

Dimensions in mm





top view



side view

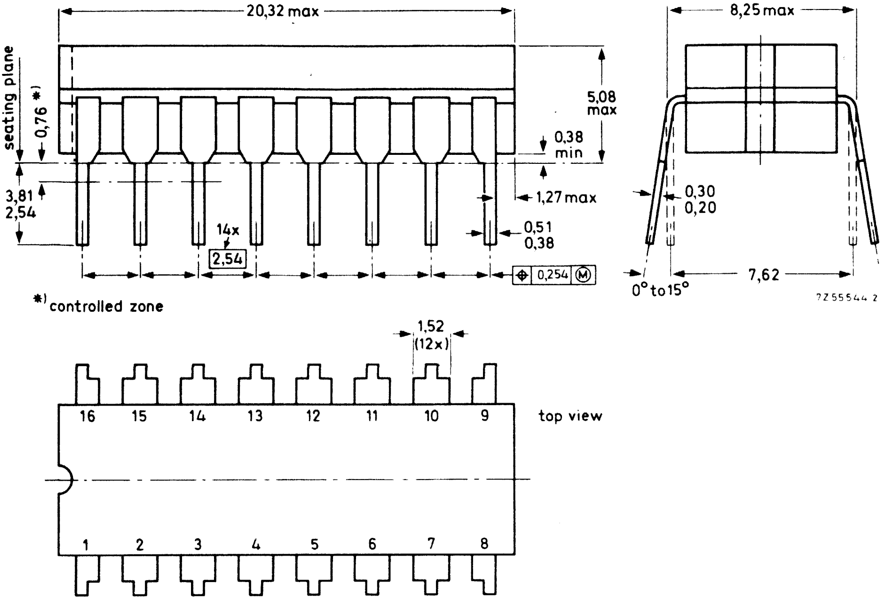
A) Centre-lines of all leads are within ±0, 127 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated

*) Pin 1 position may be identified by the presence of:
-a, b or c, or
-b and c

16 LEAD CERAMIC DUAL IN-LINE

Dimensions in mm

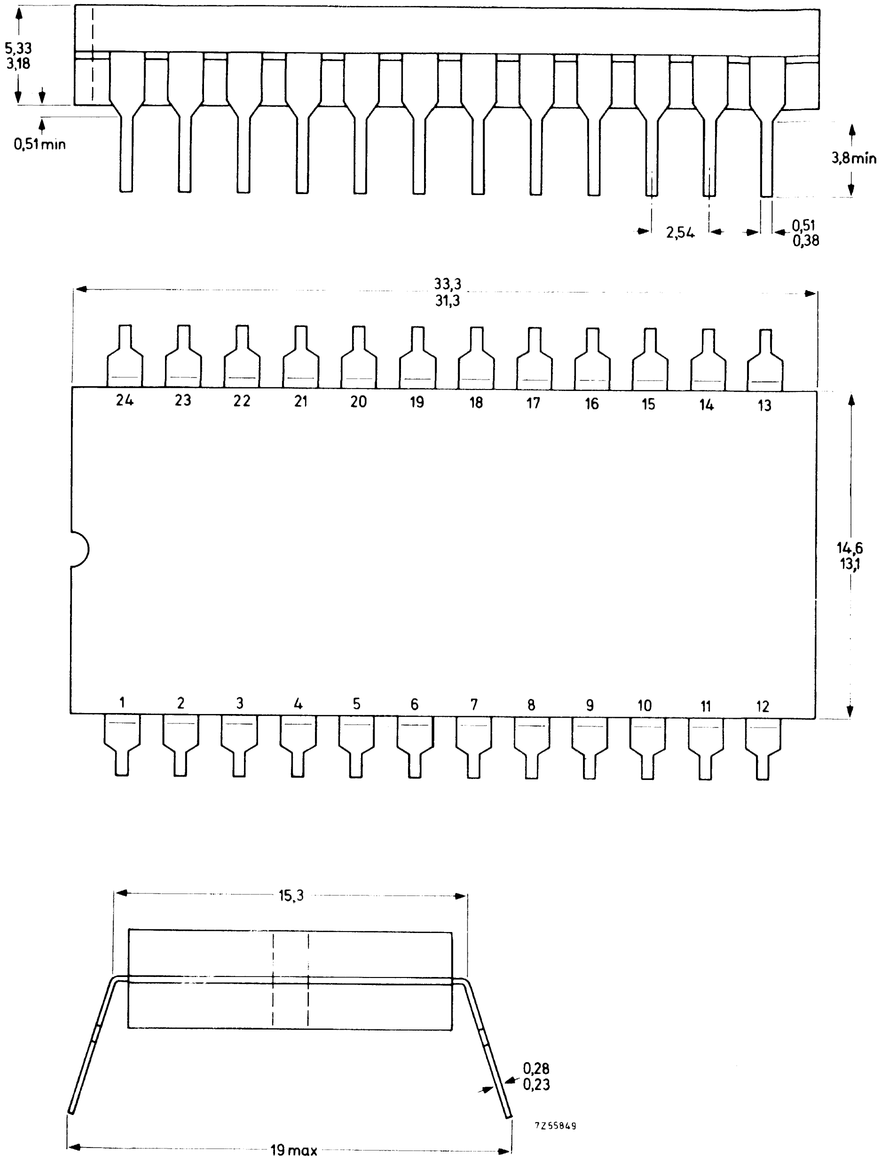


Notes

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

24 LEAD CERAMIC DUAL IN-LINE

Dimensions in mm

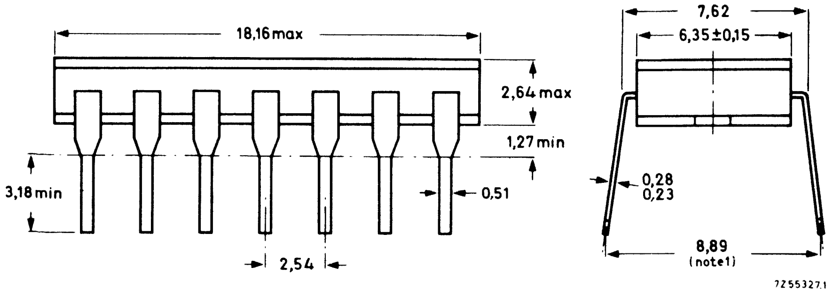


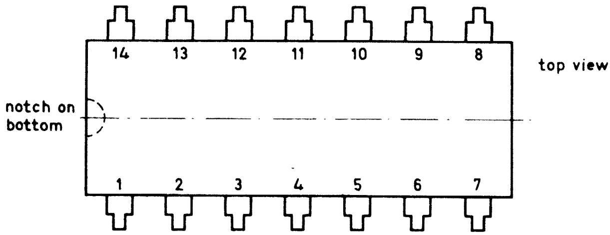
Notes

1. Leads on opposite sides are designed to fit in holes 15,24 mm apart. They are given positive misalignment so that they grip after insertion.
2. Leads are gold plated Kovar.

14 LEAD METAL-CERAMIC DUAL IN-LINE

Dimensions in mm

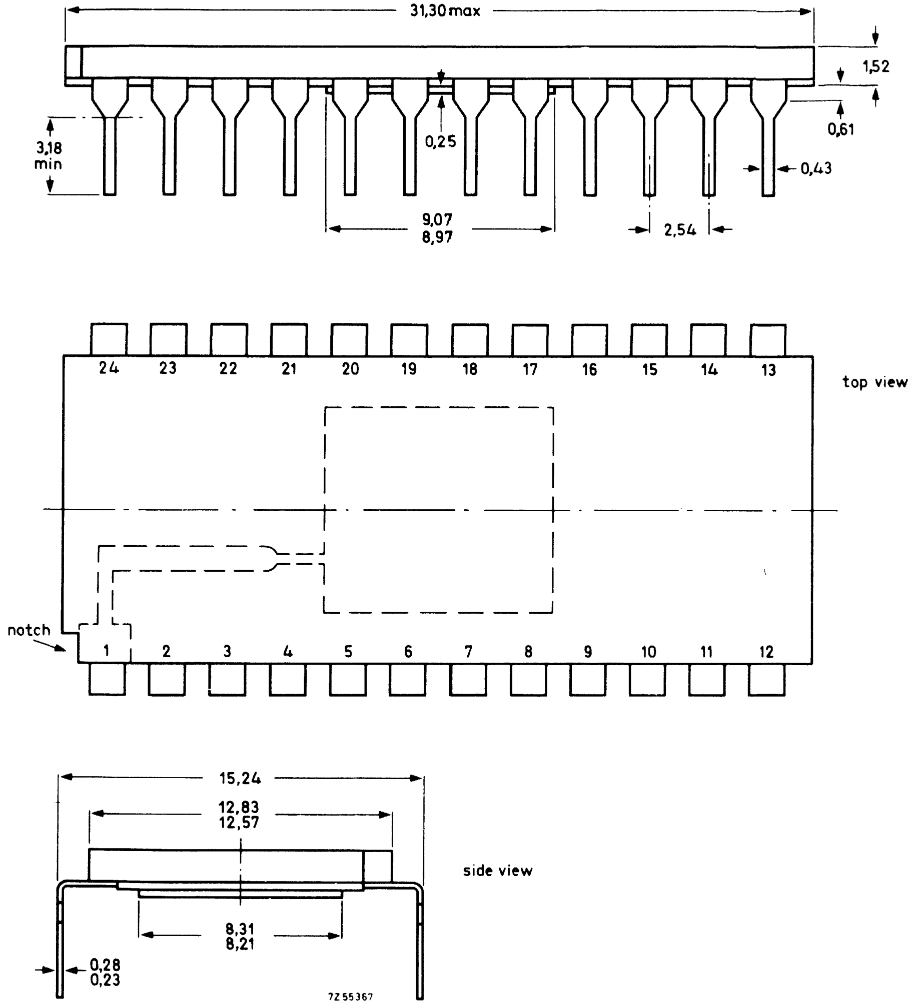




1. Leads on opposite sides are designed to fit in holes 7,62 mm apart. They are given positive misaligment so that they grip after insertion.
2. Pin 1 is normally marked by a dot.

24 LEAD METAL-CERAMIC DUAL IN-LINE

Dimensions in mm

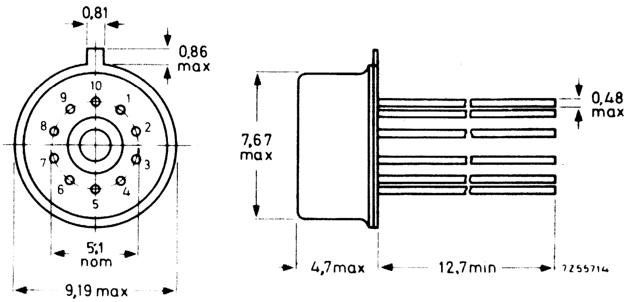


Notes

1. Leads on opposite sides are designed to fit in holes 15, 24 mm apart.
2. Pin 1 is marked by a notch and connected to the metal lid on the bottom of the package.

TO-100 METAL ENVELOPE

Dimensions in mm



Measures to be taken when handling MOS devices

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental overvoltages. In storing and handling them, the following precautions should be observed.

1. Store and transport the circuits in carriers that either short-circuit all leads or insulate all leads from external contact.

2. Work on a conductive surface (e.g. a metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, as by a metal bracelet and a conductive cord or chain. Also connect all testing and handling equipment to the surface.

3. Mount MOS integrated circuits on printed circuit boards after all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric potential (earth).
   If it is impossible to earth the printed circuit board, the person mounting the circuits should touch the board before bringing a MOS circuit into contact with it.
   The soldering iron or bath should also be kept at the same potential as the MOS circuit and the board.

4. Avoid building up electrostatic charges through movement of air over non-conductive material (plastics, ceramics). Acid sinks and test ovens call for special precautions in this regard.
   Beware of voltage surges due to:
   - switching electrical equipment on or off
   - relays
   - a.c. lines.

5. If possible, dress personnel in anti-static clothing (no wool, silk, or synthetic fibres).

N.B. Points 2 and 3 call for special attention to personnel safety.

GATE SYMBOLS

Symbols taken from MIL-STD-806B published 26-2-1962 together with the explanation given in the MIL-STD are framed (the number in brackets refers to the section of the MIL-STD from which the extract has been made).
Other symbols and explanations are unframed.

A. LOGIC SYMBOLS (5 partial)*)

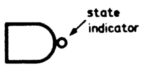
AND The symbol shown below represents the AND function (5.1).

OR The symbol shown below represents the OR function (5.2).

EXCLUSIVE-OR The symbol shown below represents the Exclusive-OR function (5.6).

STATE INDICATOR (Active) (5.3). The presence of the small circle symbol at the input(s) or output(s) of a function indicates:

(a) Input Condition. The electrical condition at the input terminal(s) which control the active state of the respective function.
(b) Output Condition. The electrical condition existing at the output terminal(s) of an activated function.



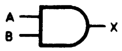
(5.3.1) A small circle(s) at the input(s) to any element (logical or non-logical) indicates that the relatively LOW (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively HIGH (H) input signal activates the function.
(5.3.2) A small circle at the symbol output indicates that the output terminal of the activated function is relatively LOW (L), the absence indicates that the output terminal is relatively HIGH (H).
This small circle shall never be drawn by itself on a diagram.

On pages 4 and 5 the terms HIGH and LOW and the translation of logic notations "0" and "1" into HIGH and LOW will be elucidated.

*) See appendix for drawing dimensions.

EXAMPLES

AND (5.1.1)



A	B	X
L	L	L
H	L	L
L	H	L
H	H	H

The output is HIGH if and only if all inputs are HIGH.

(5.4)

A	B	X
L	L	H
H	L	H
L	H	H
H	H	L

The output is LOW if and only if all inputs are HIGH

OR (5.2.1)

A	B	X
L	L	L
H	L	H
L	H	H
H	H	H

The output is HIGH if and only if any one or more of the inputs are HIGH.

(5.5)

A	B	X
L	L	H
H	L	L
L	H	L
H	H	L

The output is LOW if and only if any one or more of the inputs are HIGH.

EXCLUSIVE -OR (5.6.1)

A	B	X
L	L	L
H	L	H
L	H	H
H	H	L

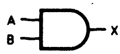
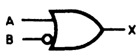
The output is HIGH if and only if any one input is HIGH and all other inputs are LOW.

A	B	X
L	L	H
H	L	L
L	H	L
H	H	H

The output is LOW if and only if any one input is HIGH and all other inputs are LOW.

Table I, (5.7) of MIL-STD-806B, shows two-input AND and OR gate symbols with all the possible combinations of terminals with or without state indicator. It will be noted that the AND-gate symbol in the 1st column has the same function table as the OR-gate symbol in the 2nd column.

Table I

AND	OR	Function Table A B | X
		H H | H H L | L L H | L L L | L
		H H | L H L | L L H | H L L | L
		H H | L H L | H L H | L L L | L
	 See note 1	H H | L H L | L L H | L L L | H
		H H | H H L | H L H | H L L | L
		H H | H H L | L L H | H L L | H
		H H | H H L | H L H | L L L | H
 See note 2		H H | L H L | H L H | H L L | H

Note 1. In literature often described as NOR.
Note 2. In literature often described as NAND.

Although the MIL-STD-806B does not use the expression NAND and NOR they are referred to becaused these terms are commonly used.

Although MIL-STD-806B shows the EXCLUSIVE-OR symbol only without state indicator, for the sake of completeness Table II shows it with all the possible combinations of terminals with or without state indicator. It will be noted from the table that one function table (3rd column) is applicable to four symbols.

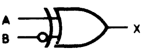
Table II

Symbol

Symbol

Function Table

A	B	X
H	H	L
H	L	H
L	H	H
L	L	L



See note 3

A	B	X
H	H	H
H	L	L
L	H	L
L	L	H

Note 3. In literature described as BINARY COMPARATOR

HIGH AND LOW

The terms relatively HIGH and relatively LOW are explained with reference to the following three examples

+5 volts = HIGH
+0.5 volts = LOW

+0.5 volts = HIGH
-5 volts = LOW

-5 volts = HIGH
-10 volts = LOW

It can be seen that the more positive voltage is termed relatively HIGH and the less positive is termed relatively LOW. These terms are abbreviated to HIGH (H) and LOW (L) respectively and are used throughout MIL-STD-806B.

LOGICAL "1" AND "0"

In deviation from MIL-STD-806B Appendix B, which for the sake of fully general systems applicability (page 17, fig.5) refrains from establishing any fixed relations between "active-nonactive" and "logical 0-1", we have in the following rules chosen to relate "active" to "1" and "non-active" to "0", as being most suitable when regarding each gate function separately.

"0" at the input always symbolizes the non-activating signal or, at the output, the signal from a non-activated gate;

"1" at the input always symbolizes the activating signal or, at the output, the signal from an activated gate. (The expression activated does not mean that current must flow at the respective terminal(s) but refers to the influence of inputs upon the output(s) of the respective gates.)

The translation from the logic notation into the electrical levels HIGH and LOW is explained with the aid of two examples, one without state indicators and one with. In each case a two-input AND gate truth table is drawn up, and a function table corresponding to the symbol is given so that a direct comparison can be made.

For inputs or outputs	without state indicator	with state indicator
	Logic 1 = HIGH (H)	Logic 1 = LOW (L)
	Logic 0 = LOW (L)	Logic 0 = HIGH (H)

EXAMPLE

Truth Table

Inputs A	Inputs B	Output X
0	0	0
1	0	0
0	1	0
1	1	1

Symbol

Function Table

Inputs A	Inputs B	Output X
L	L	L
H	L	L
L	H	L
H	H	H

Inputs A	Inputs B	Output X
0	0	0
1	0	0
0	1	0
1	1	1

Inputs A	Inputs B	Output X
H	L	H
L	L	H
H	H	H
L	H	L

B. **DRAWING PRACTICE**

Any of the symbols from Tables I and II may be used in diagrams, bearing in mind the following general rule.
Every signal line shall preferably have at each end
either a state indicator circle,
or no state indicator circle.
An example showing how compliance with this rule can be achieved is given in the following sketch.

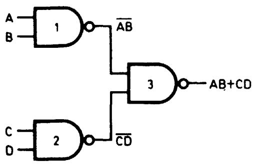


fig. 1

should be drawn as

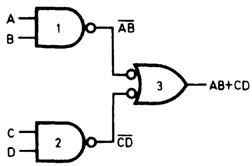


fig. 2

A further advantage of drawing the symbol of gate 3 as in fig. 2 is that it is more apparent that it behaves as an OR function than when drawn as in fig. 1 (cf. table I).

When state indicators are not used no more than four input lines should be drawn at the input side of the symbol (see fig. 3).

When state indicators are used no more than three input lines should be drawn at the input side (see fig. 4).
Following these rules will help to avoid unnecessary crowding of lines in the drawing.
When more input lines are needed the input side of the symbol can be extended in any of the ways indicated in fig. 5.

fig. 3

fig. 4

Equidistant lines

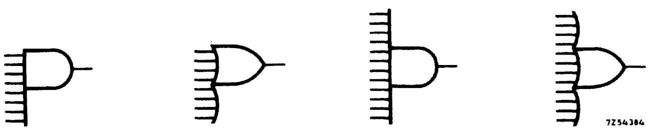


fig. 5

EXTENDED INPUTS

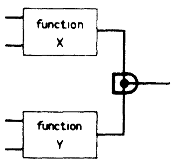
If the number of inputs to an expandable gate is extended by means of an expander circuit, the output line(s) of the expander is (are) connected to the specific expansion input(s) of the gate as drawn below.
The expander symbol shall be drawn to the same dimensions as the gate symbol; however, two filled arrows shall be drawn on each connection line, one arrow close to the expander symbol and another close to the gate symbol.

f = gate
E = expander

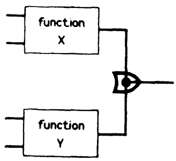
A signal line provided with arrows need not imply the usual logic levels. Generally it should not be connected to "normal" inputs or outputs of gates.

C. OUTPUT COMBINATIONS (6.3)

Where functions have the capability of being combined according to the AND (or OR) function, simply by having the outputs connected, that capability shall be shown by enveloping the branched connection with a smaller sized AND or OR symbol .



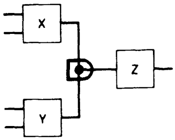
Dot "AND"



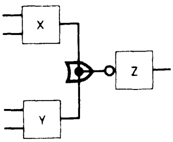
Dot "OR"

Note: These connections of outputs are often described in the literature as "WIRED-OR".

EXAMPLES



The function Z is activated on its input by a HIGH level (because a state indicator is not applied there) if and only if both outputs of functions X and Y are HIGH.
The branched connection shall therefore be enveloped by a small-sized AND symbol.

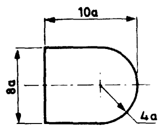


The function Z is activated on its input by a LOW level (because a state indicator is applied there) if and only if one or both outputs of the functions X and Y are LOW.
The branched connection shall therefore be enveloped by a small-sized OR symbol.
It should be noted that it would seem necessary to use state indicators on all terminals of the Dot "OR" symbol for correct interpretation of the circuit. However it is not usual to use state indicators on Dot symbols.

APPENDIX

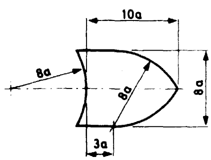
DRAWING DIMENSIONS

Ratio of dimensions of symbols may be derived from the drawings shown.

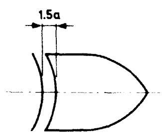


AND

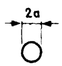
Symbols enveloping a branched connection shall have half the dimensions of the fundamental symbols.



OR



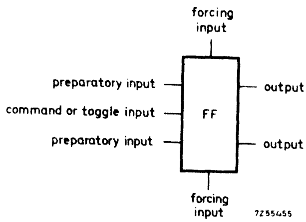
EXCLUSIVE-OR



STATE INDICATOR

FLIP-FLOP SYMBOLS

1. GENERAL SYMBOL



2. DEFINITIONS

Active or "1" state of an input signal.

That state (either a level or a transition from one level to the other) which causes, directly or indirectly, a change of the output state. Conversely, the inactive or "0" state of an input signal is that state which does not cause an output change.

Output state.

There may be one output terminal (Q) or two (Q_1 and Q_2). If there are two, the "output state" refers to the states of the signals at Q_1 and Q_2; since these are normally complementary, the state at Q_1 is usually considered to represent the output state.

Preparatory input terminal (e.g. J, K, D)

An input terminal to which application of an active signal does not directly cause a change of the output state but prepares the circuit for such a change.

Command input terminal (T)

An input terminal to which application of an active signal causes the output to assume the state corresponding to the preparatory inputs. It is also known as the "clock input terminal".

Toggle input terminal (T)

An input terminal at which an active transition from one level to the other directly causes a change of the output state.

Forcing input terminal (S_1 = "direct set", S_2 = "direct reset")

An input terminal at which application of an active signal directly causes the output to assume a specific state, irrespective of the states of other input terminals.

3. LOCATION OF TERMINALS AND USE OF POLARITY STATE INDICATOR, SHOWN BY EXAMPLES

Legend:

H = HIGH level

L = LOW level

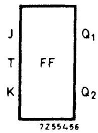
L→H = transition from LOW level to HIGH level

H→L = transition from HIGH level to LOW level

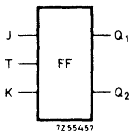
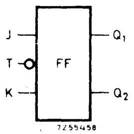
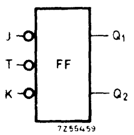
X = state (level or transition) has no influence

? = indeterminate, unless exact timing of relevant input signals (e.g. S_1 and S_2) is known.

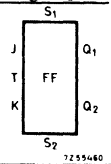
3.1. JK flip-flop without forcing inputs



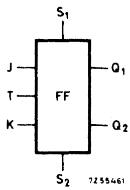
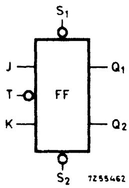
An active ("1") signal at J, together with an inactive ("0") signal at K and an active signal transition at T, causes the "1" state at Q_1 and the "0" state at Q_2.

Symbol	Function table J	K	T	Q_1 Q_2
	H	L	L→H	H L
	L	H	L→H	L H
	H	H	L→H	reversed
	L	L	L→H	no change
	X	X	H→L	no change
	H	L	H→L	H L
	L	H	H→L	L H
	H	H	H→L	reversed
	L	L	H→L	no change
	X	X	L→H	no change
	L	H	H→L	H L
	H	L	H→L	L H
	L	L	H→L	reversed
	H	H	H→L	no change
	X	X	L→H	no change

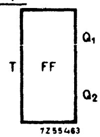
3.2. JK flip-flop with forcing inputs



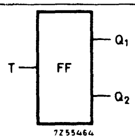
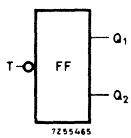
Irrespective of the states at J, K and T: an active ("1") signal at S_1, together with an inactive ("0") signal at S_2, causes Q_1 to assume the "1" and Q_2 the "0" state

Symbol	Function table						
	J	K	T	S_1	S_2	Q_1	Q_2
	X	X	X	H	L	H	L
	X	X	X	L	H	L	H
	X	X	X	H	H	?	?
	H	L	L→H	L	L	H	L
	L	H	L→H	L	L	L	H
	H	H	L→H	L	L	reversed	
	L	L	L→H	L	L	no change	
	X	X	H→L	L	L	no change	
	X	X	X	L	H	H	L
	X	X	X	H	L	L	H
	X	X	X	L	L	?	?
	H	L	H→L	H	H	H	L
	L	H	H→L	H	H	L	H
	H	H	H→L	H	H	reversed	
	L	L	H→L	H	H	no change	
	X	X	L→H	H	H	no change	

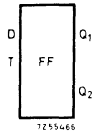
3.3. T flip-flop ("Toggle")



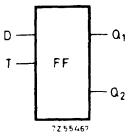
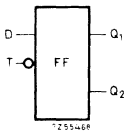
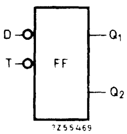
An active ("1") signal transition at T causes the complementary states at Q_1 and Q_2 to reverse.

Symbol	Function table	
	T	Q_1 Q_2
	L→H H→L	reversed no change
	H→L L→H	reversed no change

3.4. Edge-triggered D flip-flop

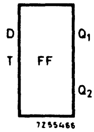


An active ("1") signal transition at T causes Q_1 to assume the same state as D. I.e., if D is in the "1" state during the active transition at T, Q_1 also assumes the "1" state: if D is "0", Q_1 also becomes "0". The output state will remain unchanged until the next active transition at T occurs.

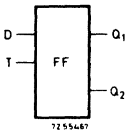
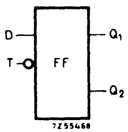
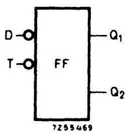
Symbol	Function table				
	D	T		Q_1	Q_2
		level	transition		
	H		L→H	H	L
	L		L→H	L	H
	X	X		no change	
	X		H→L	no change	
	H		H→L	H	L
	L		H→L	L	H
	X	X		no change	
	X		L→H	no change	
	L		H→L	H	L
	H		H→L	L	H
	X	X		no change	
	X		L→H	no change	

3.5. <u>Level-operated ("gated") D flip-flop, or "Bistable latch".</u>

(Graphical symbol equal to 3.4.)

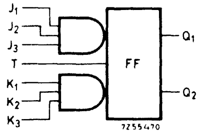


As long as the signal at T is at its active ("1") level, the signal at Q_1 follows the signal at D. When the signal at T changes to its inactive ("0") level, the signal at Q_1 latches (Subsequent changes in D cause no change in Q_1). Q_1 unlatches when the signal at T returns to its active level.

Symbol	Function table				
	D	T		Q_1	Q_2
		level	subsequent transition		
	H	H		H	L
	H	H	H→L	H	L
	L	H		L	H
	L	H	H→L	L	H
	X	L		no change	
	H	L		H	L
	H	L	L→H	H	L
	L	L		L	H
	L	L	L→H	L	H
	X	H		no change	
	L	L		H	L
	L	L	L→H	H	L
	H	L		L	H
	H	L	L→H	L	H
	X	H		no change	

4. MULTIPLE INPUTS

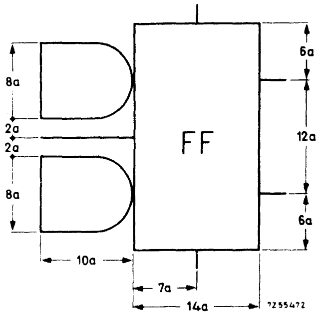
Where inputs are functionally combined by an input gate, the connecting line between the gate symbol and the flip-flop symbol may conveniently be omitted, as shown in the drawing.



5. TIME DELAY CIRCUIT

The following time delay symbol (MIL-STD-806 B, 5.15) is used in some logic flip-flop block diagrams:

6. DRAWING DIMENSIONS (to MIL-STD-806 B)



The ratio of dimensions is given in the drawing above.

For dimensions of gates and state-indicators see "Appendix", page 8.

RATING SYSTEMS

ACCORDING TO I.E.C. PUBLICATION 134

1. DEFINITIONS OF TERMS USED

1.1 Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note: This definition excludes inductors, capacitors, resistors and similar components.

1.2 Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

1.3 Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

1.4 Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note: Limiting conditions may be either maxima or minima.

1.5 Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

2. ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

p.t.o.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

3. DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

4. DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

NOTE

It is common use to apply the Absolute Maximum System in semiconductor published data.

LETTER SYMBOLS
FOR DIGITAL INTEGRATED CIRCUITS

(Additional symbols for MOS circuits on page 4)

1. General

The voltages and currents are related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a letter relating to the function of the device or the function of the pertinent signal.
In order to avoid confusion by any ambiguity in logical conventions, signal levels are indicated by H (= HIGH, for the more positive potential) and L (= LOW, for the less positive potential). Where circuit functions or logical equations are involved, the logical convention is mentioned specifically (for positive logic: H = 1, and for negative logic: H = 0).

2. Terminal designations

D = D input of D type latch flip-flops
E = expander input (if necessary, this letter may be followed by an index, e.g. E_1 or E_2 or by one of the input letters, such as EG = gate expander input)
G = gate input
J, K = J, K input of JK flip-flops
N = negative supply
P = positive supply
Q = output
S = direct SET input
T = trigger (or toggle) input
Ø = common supply return and voltage reference

3. Subscript sequence for voltages and currents

First subscript : terminal designation letter.
Second subscript: H (for HIGH) or L (for LOW), if applicable.
Third subscript : min or max, if applicable.
Examples: V_P, I_{QL}, V_{QHmin}, I_{PH} (in the latter case H denotes that the output level is HIGH).

4. Polarity of current and voltage

A current is defined as positive when its conventional direction of flow is into the device.
Unless otherwise specified, a voltage is measured with respect to the reference terminal (Ø). Its polarity is defined as positive when the potential is higher than that of the reference terminal.

5. Time designations

If required for reasons of unambiguity, the related terminals may be included in the designations given below (e.g. t_{fQ1}).

t_f = fall time (transition from HIGH to LOW, see Fig. 1)

t_H = signal HIGH duration (Fig. 1)

t_L = signal LOW duration (Fig. 1)

t_{pd} = average propagation delay time, defined as $\frac{t_{pdr} + t_{pdf}}{2}$

t_{pdf} = fall propagation delay time (output voltage falling, see Fig. 2)

t_{pdr} = rise propagation delay time (output voltage rising, see Fig. 2)

t_r = rise time (transition from LOW to HIGH, see Fig. 1)

t_{sc} = duration of short circuit (from relevant terminal to common return terminal)

V_{pd} = reference voltage level for propagation delay measurement

Fig. 1.

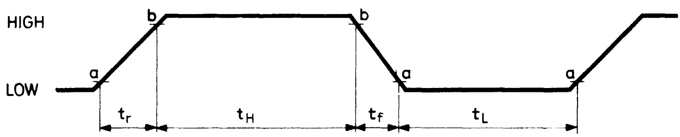
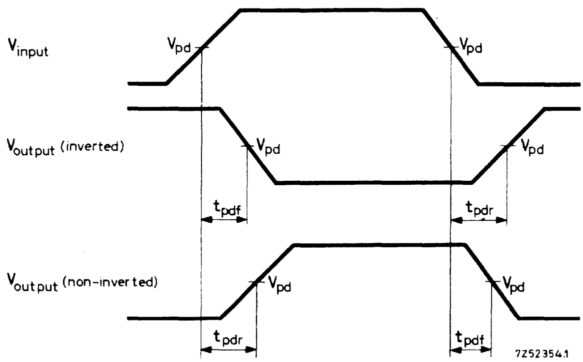


Fig. 2.



6. Other designations

i.c. = internally connected
Terminals with this indication should be left open. Otherwise correct working cannot be ensured; the device may even be damaged

n.c. = not connected internally
It is recommended not to use these terminals for any connection

I_P = supply current
The logic state of the device indicated by H or L is normally referred to the output level, unless otherwise specified

I_{Pmax} = supply current
Maximum d.c. value under defined conditions

M = d.c. noise margin

M_L = d.c. noise margin, signal level LOW
(defined as: $M_L = V_{GLmax} - V_{QLmax}$ under defined loading, temperature and supply voltage conditions)

M_H = d.c. noise margin, signal level HIGH
(calculated from: $M_H = V_{QHmin} - V_{GHmin}$ under defined loading, temperature and supply voltage conditions)

N_a = available d.c. fan-out (defined as: $N_a = \frac{I_{QLmax}}{-I_{GLmax}}$ under defined temperature and supply voltage conditions)

P_H, P_L = power consumption, defined as the product of the supply current(s) and of the corresponding supply voltage(s). The logical state of the device, indicated by a letter index H or L, is normally referred to the output level, unless otherwise specified

P_{av} = average power consumption at 50% duty cycle, unless otherwise specified. It is defined as: $P_{av} = V_P \cdot \frac{I_{PH} + I_{PL}}{2}$

P_{tot} = power dissipation, defined as the total power dissipated by the device. It is the sum of the products of all currents and voltages at each of the input, output and supply terminals, their polarities being taken into account. The logical state of the device indicated by a letter index H or L is normally referred to the output level, unless otherwise specified

T_{amb} = operating ambient temperature, i.e. the temperature of the free air in which the normally operating device is placed without external heat conduction, unless otherwise specified

T_{stg} = storage temperature, i.e. the temperature of the ambient medium in which the non-operating device is stored

V_{GLmax} = input voltage LOW at terminal G. With the specified level applied to the input of an inverting gate the output level will not be lower than the specified value V_{QHmin} at given I_{QH}.

V_{GHmin} = input voltage HIGH at terminal G. With the specified level applied to the input of an inverting gate the output level will not exceed the specified value V_{QLmax} at given I_{QL}.

ΔV_Q = change of output voltage caused by a specified change of output current

ADDITIONAL SYMBOLS FOR MOS CIRCUITS

2a. Terminal designations

I = shift register input
A = address input or decode matrix input
ϕ = clock input
WC = write control input
D = data input
CD = chip disable input
Q = output
C = chip inhibit input
P_O = common supply return and voltage reference
P_1, P_2, etc. = supply input

3a. Subscript sequence for voltages
First (with or without second) subscript: terminal designation
Second or third subscript: H (HIGH) or L (LOW) if applicable

5a. Time designations

Details are described in the data sheets

6a. Other designations

M_L = d.c. noise margin LOW ($M_L = V_{input\ L\ max} - V_{output\ L\ max}$)
M_H = d.c. noise margin HIGH($M_H = V_{output\ H\ min} - V_{input\ H\ min}$)
R_{QH} = output resistance HIGH
R_{QL} = output resistance LOW
P_{av} = average power consumption

DTL FC family

FCH101	single 8-input NAND gate, without R_c
FCH111	single 8-input NAND gate, with R_c
FCH121	dual 4-input NAND gate, without R_c
FCH131	dual 4-input NAND gate, with R_c
FCH141	triple 3-3-2-input NAND gate, without R_c
FCH151	triple 3-input NAND gate, without R_c
FCH161	triple 3-3-2-input NAND gate, with R_c
FCH171	triple 3-input NAND gate, with R_c
FCH181	quadruple 2-input NAND gate, without R_c
FCH191	quadruple 2-input NAND gate, with R_c
FCH201	sextuple INVERTER, without R_c
FCH211	sextuple INVERTER, with R_c
FCH221	dual 3-input LINE DRIVER NAND gate
FCH231	dual 4-input LINE DRIVER NAND gate
FCH281	single 5-bit COMPARATOR
FCH291	single 10-bit PARITY CHECKER
FCH301	single 4-bit DECODER
FCH311	sextuple expandable INVERTER, without R_c
FCH321	sextuple expandable INVERTER, with R_c
FCJ101	single JK FLIP-FLOP
FCJ111	single JK master-slave FLIP-FLOP
FCJ121	dual JK master-slave FLIP-FLOP
FCJ131	dual JK master-slave FLIP-FLOP
FCJ141	single asynchronous 10-COUNTER
FCJ191	dual JK master-slave FLIP-FLOP (common set input; separate reset inputs)
FCJ201	single JK master-slave FLIP-FLOP (AND inputs)
FCJ211	dual JK master-slave FLIP-FLOP (common clock input and common set input; separate reset inputs)
FCJ221	quadruple latch FLIP-FLOP (common clock input and common set input)
FCK111	monostable MULTIVIBRATOR
FCL101	level DETECTOR
FCY101	triple gate EXPANDER

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

NAND GATES

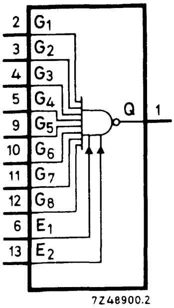
	non-R_c	R_c
Single 8-input NAND gate	FCH101	FCH111
Dual 4-input NAND gate	FCH121	FCH131
Triple 3-3-2-input NAND gate	FCH141	FCH161
Triple 3-input NAND gate	FCH151	FCH171
Quadruple 2-input NAND gate	FCH181	FCH191
Sextuple inverter	FCH201	FCH211

QUICK REFERENCE DATA

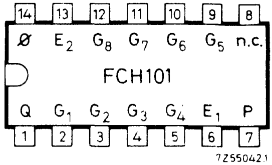
Supply voltage	V_P		6.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C	t_{pd}	typ.	30	ns
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	≥	8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ.	1.2	V
Power consumption per gate 50% duty cycle, T_{amb} = 25 °C non-R_c gate	P_{av}	typ.	7	mW
R_c gate	P_{av}	typ.	11	mW

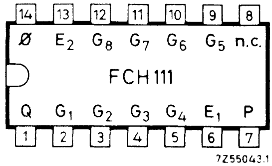
The FC family includes twelve NAND packages offering a wide selection of circuit configurations. It includes gate types with as well as without a collector resistor, ensuring optimum equipment design.
The fan-in of the circuits can easely be expanded by means of a diode array.
The outputs of these gates may be interconnected to perform the AND-OR-NOT function.

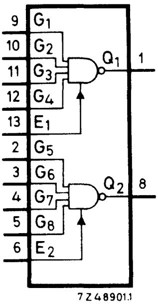
PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)



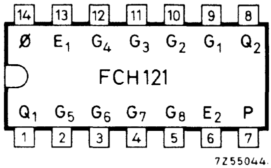
FCH101 (non-R_C)
FCH111 (R_C)

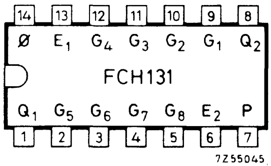


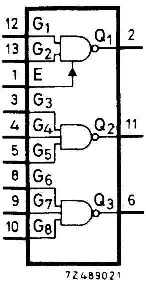




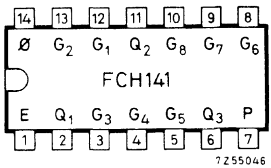
FCH121 (non-R_C)
FCH131 (R_C)

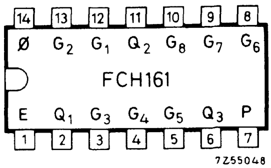


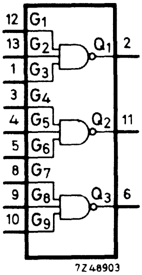


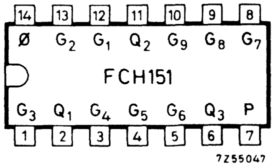


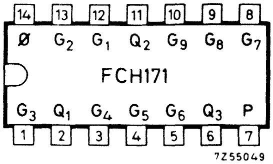
FCH141 (non-R_C)
FCH161 (R_C)



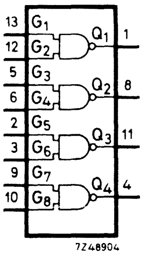


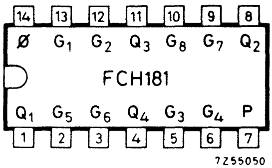


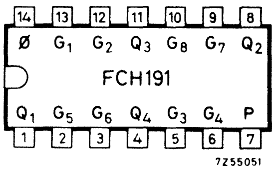




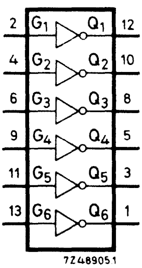
FCH151 (non-R_C)
FCH171 (R_C)

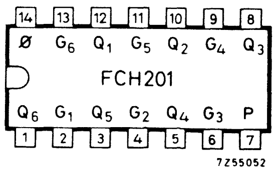


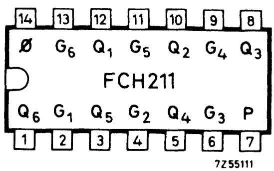




FCH181 (non-R_C)
FCH191 (R_C)



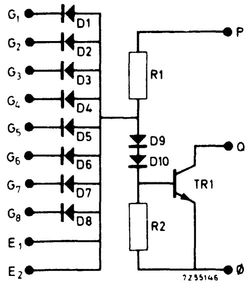




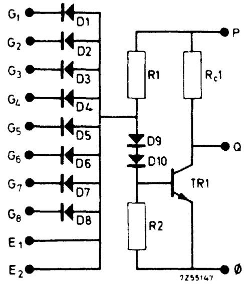
FCH201 (non-R_C)
FCH211 (R_C)

CIRCUIT DIAGRAMS

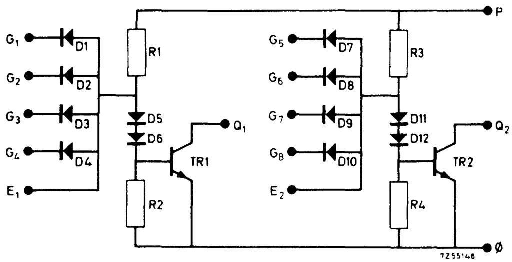
FCH101



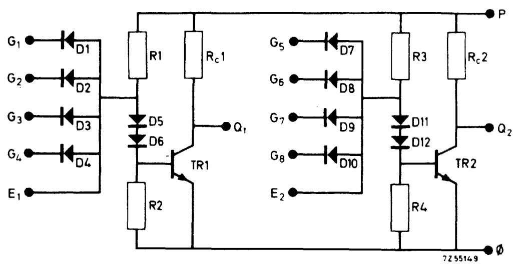
FCH111



FCH121

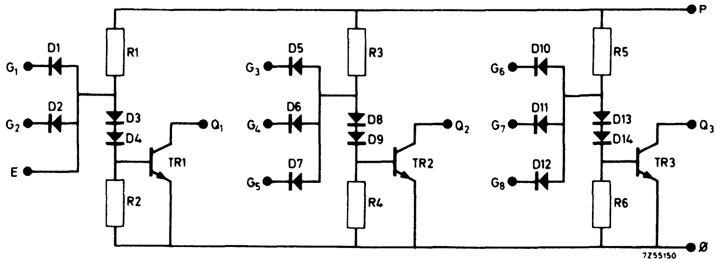


FCH131

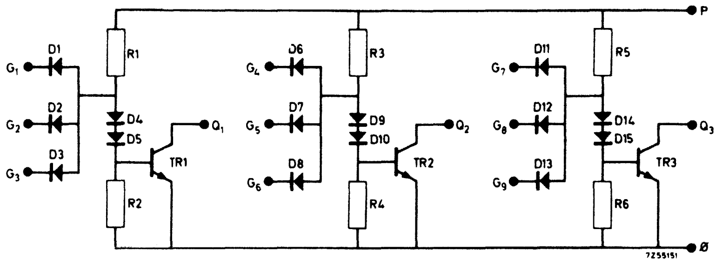


CIRCUIT DIAGRAMS (continued)

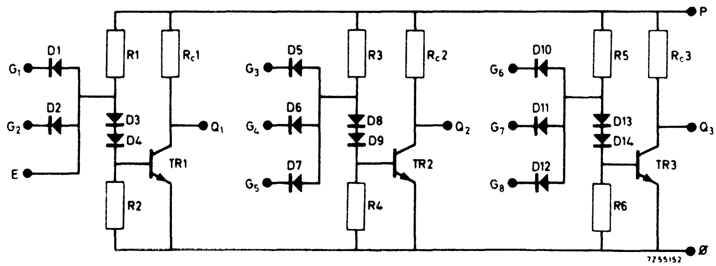
FCH141



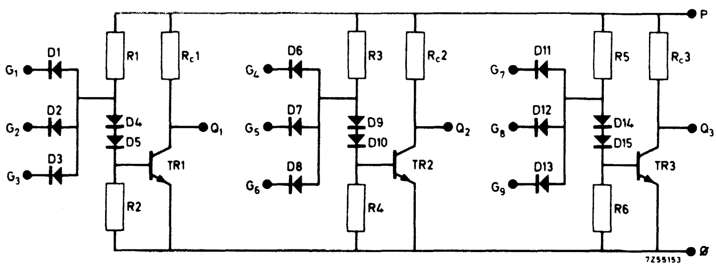
FCH151



FCH161

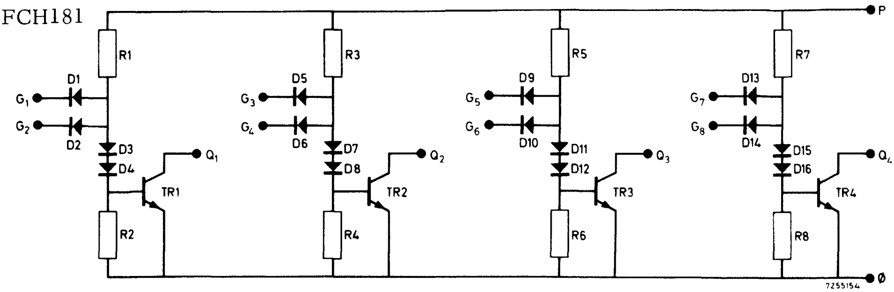


FCH171

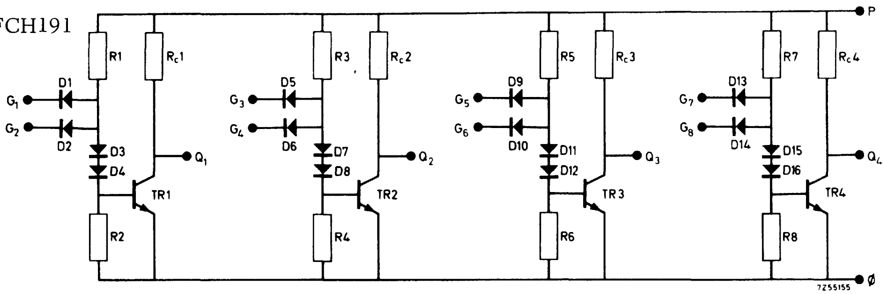


CIRCUIT DIAGRAMS (continued)

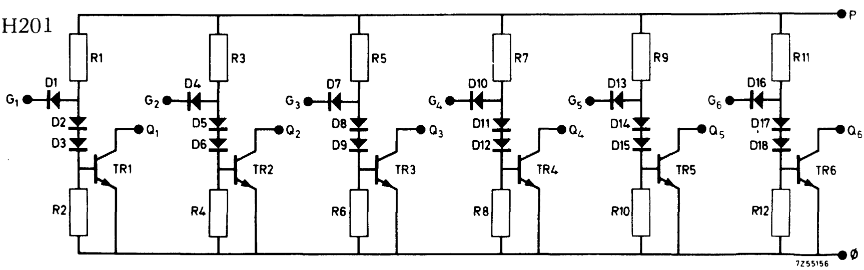
FCH181



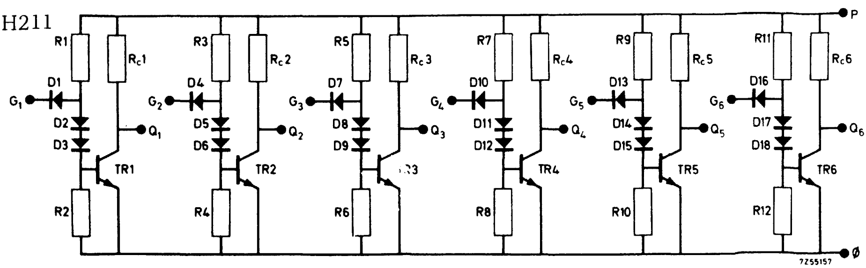
FCH191



FCH201

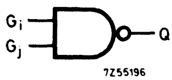


FCH211



LOGIC FUNCTION

1. Individual gate operation

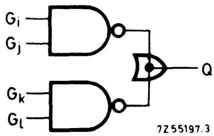


Function table

G_i	G_j	Q
L	X	H
X	L	H
H	H	L

$Q = \overline{G_i \,.\, G_j}$ for positive logic

2. Commoned gate operation



Function table

G_i	G_j	G_k	G_l	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

$Q = (\overline{G_i . G_j}) \,.\, (\overline{G_k . G_l}) = \overline{(G_i . G_j) + (G_k . G_l)}$ for positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

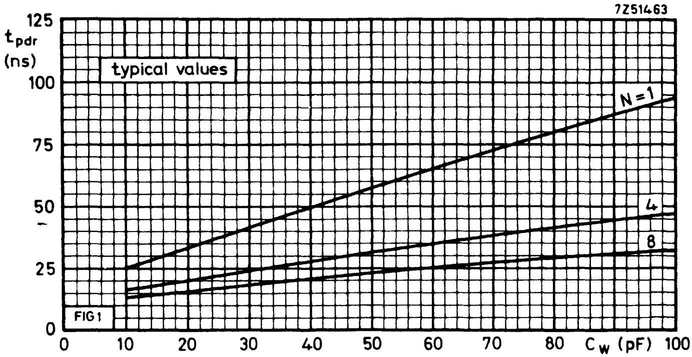
RATINGS (Limiting values) [1])

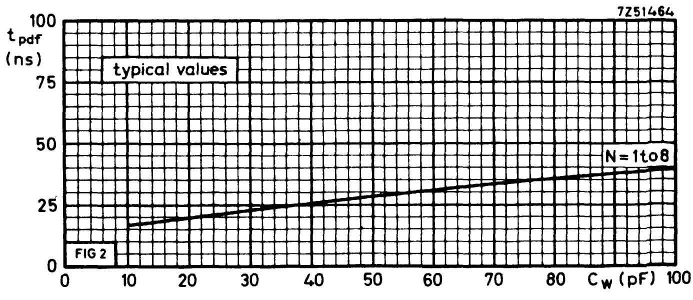
Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current [2])	$-I_Q$	max.	20	mA
Input current [3])	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Expander input voltages				
with respect to supply	$V_P - V_E$	max.	8.0	V
with respect to other inputs	$V_G - V_E$	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

[1]) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
[2]) For negative output voltage.
[3]) At this limit, input voltage type.: −1.5 V.

SYSTEM DESIGN DATA (both non-R_c and R_c)

Uniform system temperature		T_{amb}	0 to +75	°C
Uniform system supply voltage		V_P	5.7 to 6.3	V
Available d.c. fan out		N_a	≥ 8	
D.C. noise margin		M_L	min. 0.4	V
		M_H	min. 1.8	V
Average propagation delay time		t_{pd}	max. 75	ns
Equivalent input capacitance		C_G	typ. 4	pF
Equivalent output capacitance		C_Q	typ. 10	pF
Supply current per gate	non-R_c	I_{Pav}	typ. 1.20	mA
(duty cycle 50%)	R_c	I_{Pav}	typ. 1.75	mA
Power dissipation at T_{amb} = 75 °C	non-R_c	P_{tot}	max. 17.5	mW
(each gate)	R_c	P_{tot}	max. 22	mW





CHARACTERISTICS of non-R_C gates

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	16.0 18.0	15.1 17.0	14.2 16.0	mA mA	5.7 6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	V_G = 0.4 V; other inputs floating
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Output current HIGH	I_{QHmax}	70	70	70	μA	5.7 and 6.3	V_Q = 5.3 V
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Supply current 1)	I_{Pmax}	2.0	1.9	1.8	mA	6.3	G inputs LOW
DYNAMIC DATA							
Rise propagation delay time	t_{pdrmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdrmax}	-	70	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF
Fall propagation delay time	t_{pdfmax}	-	65	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdfmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF

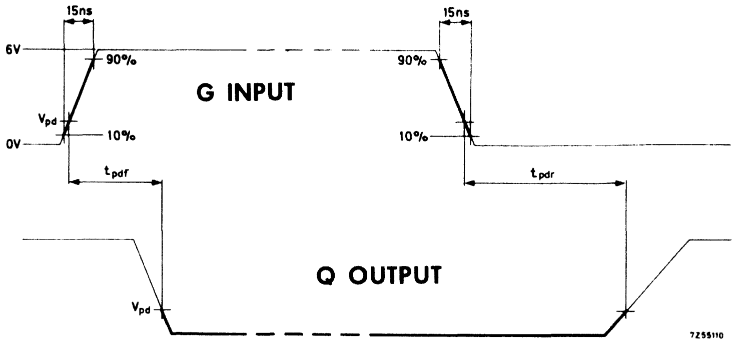
1) per gate

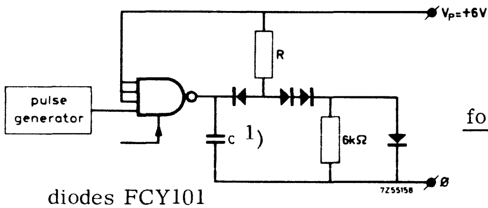
CHARACTERISTICS of R_c-gates

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	13.2 15.2	12.4 14.4	mA mA	5.7 6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
Output voltage HIGH	V_{QHmin}	5.3 4.1	5.3 4.1	5.3 3.9	V V	5.7 5.7	I_Q = 0 I_Q = −200 μA
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	V_G = 0.4 V; other inputs floating
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Output current LOW (AND-OR-NOT function)	$-I_{QLLmax}$	2.2	2.1	2.0	mA	6.3	V_G = V_{QLmax} Output forced LOW externally to V_Q = 0.4 V
Supply current	I_{Pmax}	4.2	3.8	3.6	mA	6.3	G inputs HIGH
DYNAMIC DATA							
Rise propagation delay time	t_{pdrmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdrmax}	-	70	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF
Fall propagation delay time	t_{pdfmax}	-	65	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdfmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF

CHARACTERISTICS (continued)

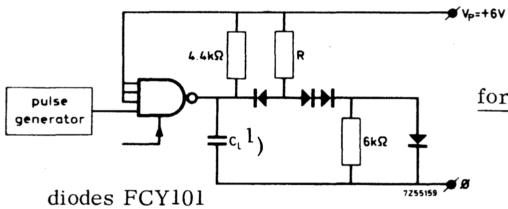
DYNAMIC DATA





for R_C gates

diodes FCY101



for non-R_C gates

diodes FCY101

Waveforms and loading circuits, illustrating measurement of t_{pdr} and t_{pdf}.

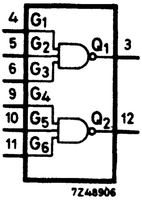
Equivalent load for N = 1 and C_L = 40 pF when R = 4 kΩ

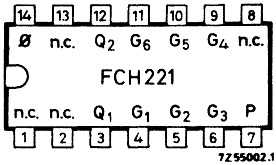
N = 6 and C_L = 60 pF when R = 670 Ω

[1]) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL 3-INPUT LINE DRIVER NAND GATE



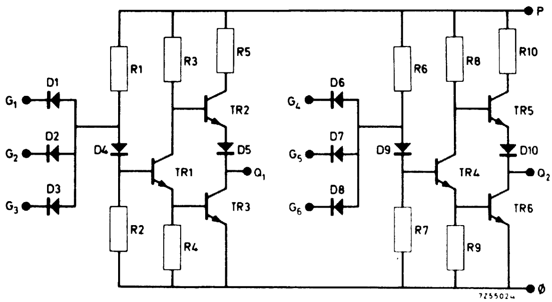


QUICK REFERENCE DATA				
Supply voltage	V_P		6.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay time N = 15, C_w = 250 pF, T_{amb} = 25 °C	t_{pd}	typ.	35	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	≥	14	
D.C. noise margin T_{amb} = 25 °C	M_L	typ.	1.2	V
Power consumption per gate 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ.	11	mW

The FCH221 comprises two independent NAND gates incorporating bi-directional output circuitry for achieving high fan-out and for driving large capacitive loads. Typical applications are in parallel setting of registers, shift pulse driving and driving of long lines.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

G1 G4	G2 G5	G3 G6	Q1 Q2
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

$$Q_1 = \overline{G_1 \cdot G_2 \cdot G_3}$$
$$Q_2 = \overline{G_4 \cdot G_5 \cdot G_6}$$
for positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) [1])

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current [2])	$-I_Q$	max.	20	mA
Input current [3])	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}		-55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C
Output short-circuit duration; duty cycle 10% (either output, or both)	t_{Qsc}	max.	60	ms

[1]) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
[2]) For negative output voltage in LOW state
[3]) At this limit input voltage typ.: −1.5V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out	N_a	⩾	14	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	1.1	V
Average propagation delay time	t_{pd}	max.	113	ns
Equivalent input capacitance	C_G	typ.	7	pF
Supply current (duty cycle 50 %) [1]	I_{Pav}	typ.	3.6	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	65	mW

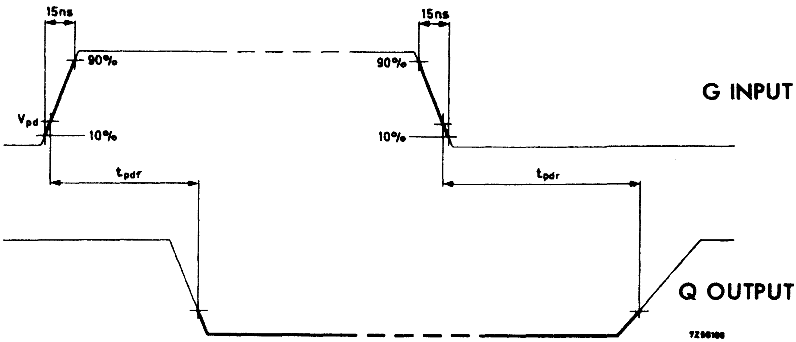
[1]) Both gates together; outputs not short-circuited.

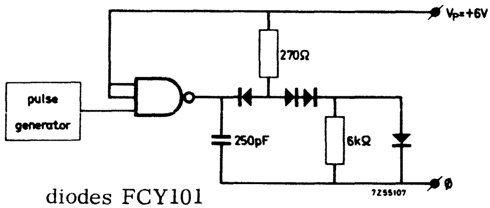
CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	25 28	27 27	26 26	mA mA	5.7 6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
Output voltage HIGH	V_{QHmin}	3.4 2.2	3.6 2.5	3.9 2.9	V V	5.7 5.7	I_Q = −30 μA I_Q = −5 mA
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	V_G = 0.4 V; other inputs floating
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	$V_G = V_{QHmin}$ other inputs 0 V
Output short circuit current	$-I_{Qsc}$	16.5	19.5	18.0	mA	5.7	$V_G = V_{GLmax}$ V_Q = 0 V
Supply current (both gates together)	I_{Pmax}	–	7.5	–	mA	6.3	G inputs HIGH
DYNAMIC DATA							
Rise propagation delay time	$t_{pdr\,max}$	130	105	130	ns	6.0	V_{pd} = 1.5 V N = 15; C_L = 250 pF
Fall propagation delay time	$t_{pdf\,max}$	95	80	95	ns	6.0	V_{pd} = 1.5 V N = 15; C_L = 250 pF

CHARACTERISTICS (continued)

DYNAMIC DATA





diodes FCY101

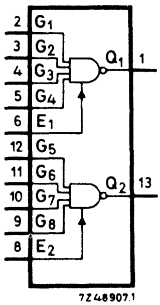
Equivalent load for N = 15 and C_L [1]) = 250 pF

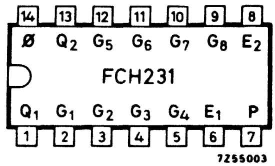
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL 4-INPUT LINE DRIVER NAND GATE



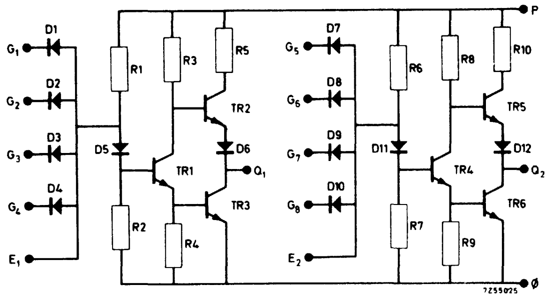


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 20, C_W = 250 pF, T_{amb} = 25 °C	t_{pd}	typ. 35	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 20	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption per gate 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 11	mW

The FCH231 comprises two independent NAND gates incorporating bi-directional output circuitry for achieving very high fan-out and for driving large capacitive loads. Typical applications are in parallel setting of registers, shift pulse driving and driving of long lines.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A).(See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

G_1 / G_5	G_2 / G_6	G_3 / G_7	G_4 / G_8	Q_1 / Q_2
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

$$Q_1 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot E_1}^{\,*}$$
$$Q_2 = \overline{G_5 \cdot G_6 \cdot G_7 \cdot G_8 \cdot E_2}^{\,*}$$
} for positive logic

* When provided with diode

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Expander input voltages				
with respect to supply	$V_P - V_E$	max.	8.0	V
with respect to other inputs	$V_G - V_E$	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C
Output short-circuit duration; duty cycly 10% (either output, or both)	t_{Qsc}	max.	60	ms

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out	N_a	⩾	20	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	1.2	V
Average propagation delay time	t_{pd}	max.	113	ns
Equivalent input capacitance	C_G	typ.	7	pF
Supply current (duty cycle 50%) [4]	I_{Pav}	typ.	3.6	mA
Power dissipation at T_{amb} = 75 °C [4]	P_{tot}	max.	73	mW

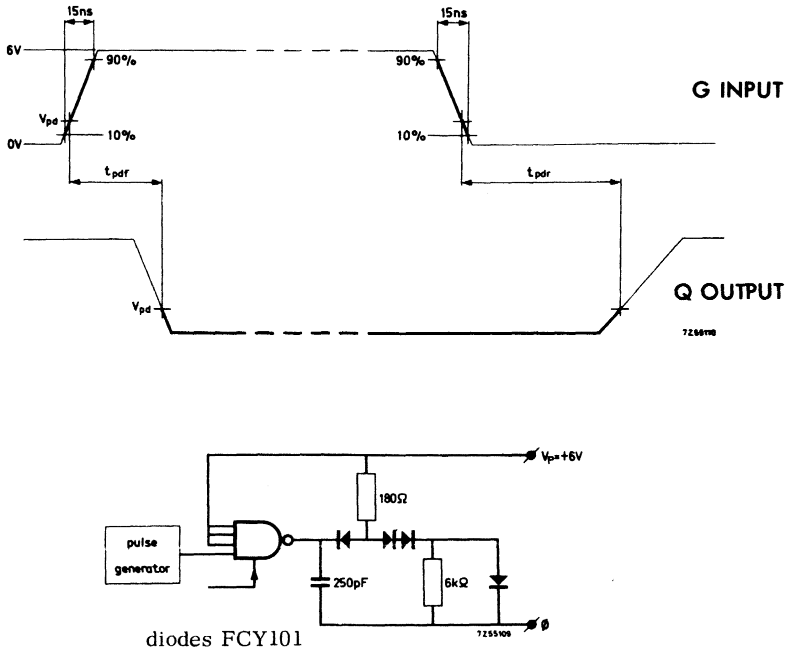
[1]) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
[2]) For negative output voltage in LOW state.
[3]) At this limit, input voltage typ. : −1.5V.
[4]) Both gates together; outputs not short-circuited.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	35	33	31	mA	5.7	
		40	38	36	mA	6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
Output voltage HIGH	V_{QHmin}	3.5	3.7	4.0	V	5.7	I_Q = −30 μA
		2.6	2.8	2.9	V	5.7	I_Q = −5 mA
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75	1.65	1.55	mA	5.7	V_G = 0.4 V; other inputs floating
		2.0	1.9	1.8	mA	6.3	
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	$V_G = V_{QHmin}$ other inputs 0 V
Output short circuit current	$-I_{Qscmin}$	16.5	19.5	18.0	mA	5.7	$V_G = V_{GLmax}$ V_Q = 0 V
Supply current (both gates together)	I_{Pmax}	–	7.5	–	mA	6.3	G inputs HIGH
DYNAMIC DATA							
Rise propagation delay time	$t_{pdr\,max}$	80	85	120	ns	6.0	V_{pd} = 1.5 V N = 20; C_L = 250 pF
Fall propagation delay time	$t_{pdf\,max}$	55	50	55	ns	6.0	V_{pd} = 1.5 V N = 20; C_L = 250 pF

CHARACTERISTICS (continued)

DYNAMIC DATA



diodes FCY101

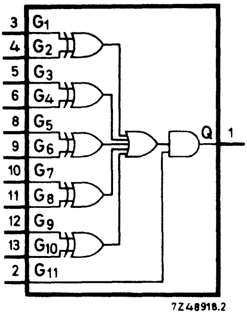
Equivalent load for N = 20 and C_L [1]) = 250 pF

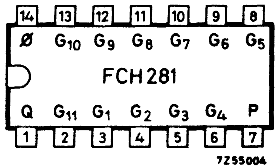
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

[1]) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 5-BIT COMPARATOR



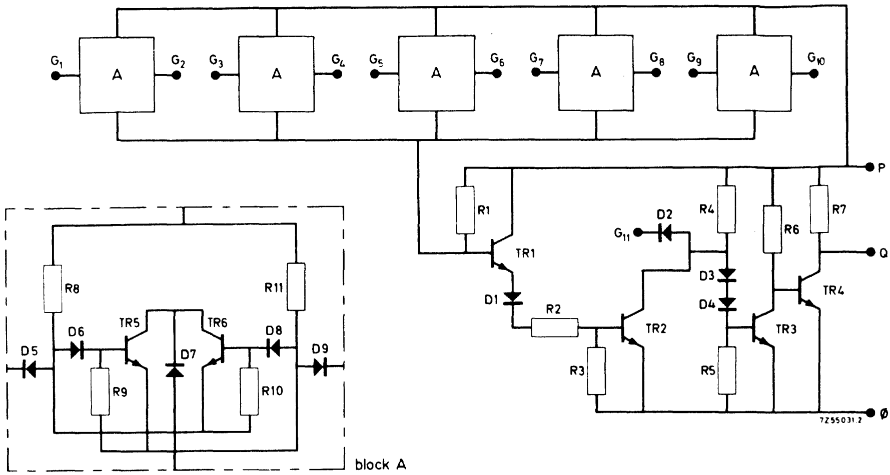


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C	t_{pd}	typ. 150	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 50	mW

The FCH281 comprises five exclusive-OR functions, an OR gate, and an AND gate. If on one or more pairs (G_1-G_2, --- G_9-G_{10}) one input is LOW and the other HIGH then the output will be HIGH provided G_{11} is HIGH. Otherwise the output will be LOW.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLE

$G_1 G_2$	$G_3 G_4$	$G_5 G_6$	$G_7 G_8$	$G_9 G_{10}$	G_{11}	Q
Equal	Equal	Equal	Equal	Equal	H	L
Unequal	X	X	X	X	H	H
X	Unequal	X	X	X	H	H
X	X	Unequal	X	X	H	H
X	X	X	Unequal	X	H	H
X	X	X	X	Unequal	H	H
X	X	X	X	X	L	L

G_1	G_2	
L	L	Equal
L	H	Unequal
H	L	Unequal
H	H	Equal

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

LOGIC FUNCTION (continued)

$$Q = \Big[\overline{(\overline{G}_1 \cdot \overline{G}_2 + G_1 \cdot G_2)} + \overline{(\overline{G}_3 \cdot \overline{G}_4 + G_3 \cdot G_4)} + \overline{(\overline{G}_5 \cdot \overline{G}_6 + G_5 \cdot G_6)} +$$

$$+ \overline{(\overline{G}_7 \cdot \overline{G}_8 + G_7 \cdot G_8)} + \overline{(\overline{G}_9 \cdot \overline{G}_{10} + G_9 \cdot G_{10})}\Big] \cdot G_{11}.$$

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current	$-I_Q$	max.	20	mA[1])
Input current	$-I_G$	max.	20	mA[2])
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

1) For negative output voltage.
2) At this limit input voltage typ. : −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out	N_a	⩾	8	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	250	ns
Equivalent input capacitance	C_G	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	10	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	90	mW

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		V_P (V)	Conditions and references
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	see note 1
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	see note 1
		16.0	15.2	14.4	mA	6.3	see note 1
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7 and 6.3	I_Q = 0 (see note 1)
	V_{QHmin}	4.7	4.7	4.5	V	5.7	I_Q = −200 µA
Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input voltage HIGH	V_{GHmin}	3.0	2.8	2.5	V	5.7 and 6.3	
Input current LOW	$-I_{G1\ to\ 10\ Lmax}$	1.75	1.65	1.55	mA	5.7	$V_{G1\ to\ 10}$ = 0.4 V
	$-I_{G1\ to\ 10\ Lmax}$	2.0	1.9	1.8	mA	6.3	$V_{G1\ to\ 10}$ = 0.4 V
	$-I_{G11\ Lmax}$	1.2	1.1	1.05	mA	5.7	V_{G11} = 0.4 V
	$-I_{G11\ Lmax}$	1.35	1.25	1.20	mA	6.3	V_{G11} = 0.4 V
Input current HIGH	I_{GHmax}	1.0	1.0	25	µA	5.7	V_G = 5.3 V other inputs 0 V
Supply current	I_{Pmax}	15.3	14.5	13.5	mA	6.3	G inputs LOW

Note 1

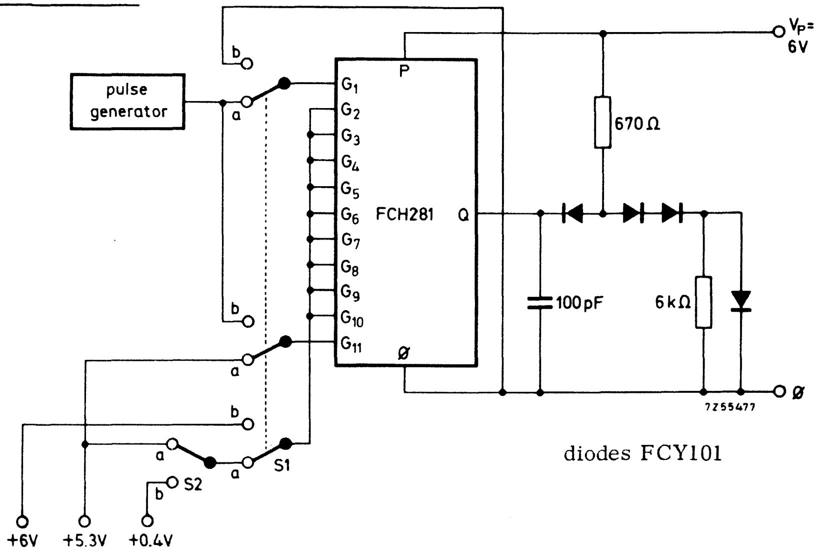
For the proper combination of inputs to be HIGH or LOW see function table on page 2.

CHARACTERISTICS (continued)

		T_{amb} (°C) 0	+25	+75		V_P (V)	Conditions and references	Fig.
DYNAMIC DATA								
Propagation delay times from one G (G_1 to G_{10}) to Q								
Rise propagation delay time	t_{pdrmax}	–	200	–	ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 80 pF all other inputs (including G_{11}) at V_G = 5.3 V	1; 2
Fall propagation delay time	t_{pdfmax}	–	200	–	ns	6.0		
Rise propagation delay time	t_{pdrmax}	–	250	–	ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 80 pF all other inputs (excluding G_{11}) at V_G = 0.4 V V_{G11} = 5.3 V	1; 3
Fall propagation delay time	t_{pdfmax}							
Propagation delay times from G_{11} to Q								
Rise propagation delay time	t_{pdrmax}	–	100	–	ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 80 pF V_{G1} = 0 V all other inputs at V_G = 6.0 V	1; 3
Fall propagation delay time	t_{pdfmax}	–	120	–	ns	6.0		

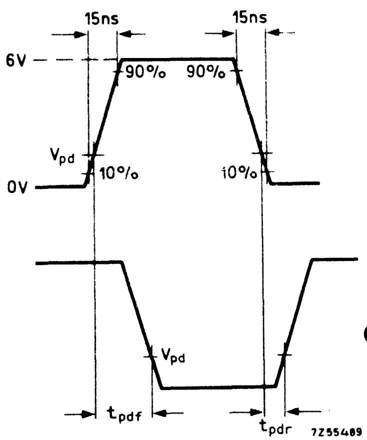
CHARACTERISTICS (continued)

DYNAMIC DATA



diodes FCY101

Fig. 1 Equivalent load for N = 6; C_L [1]) = 80 pF



INPUT

OUTPUT

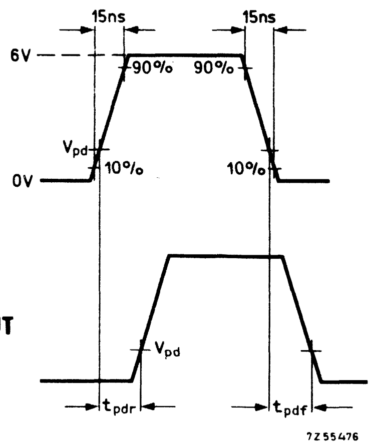


Fig. 2 Switch S1 in position a
Switch S2 in position a

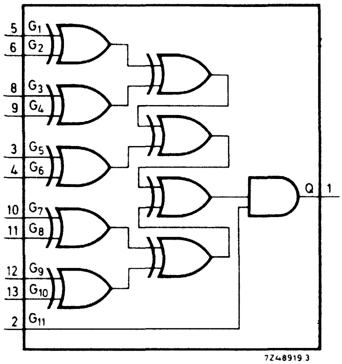
Fig. 3 Switch S1 in position a
Switch S2 in position b
or
Switch S1 in position b
Switch S2 immaterial

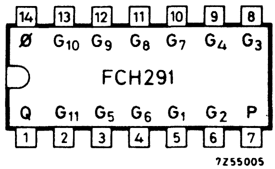
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

1) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 10-BIT PARITY CHECKER



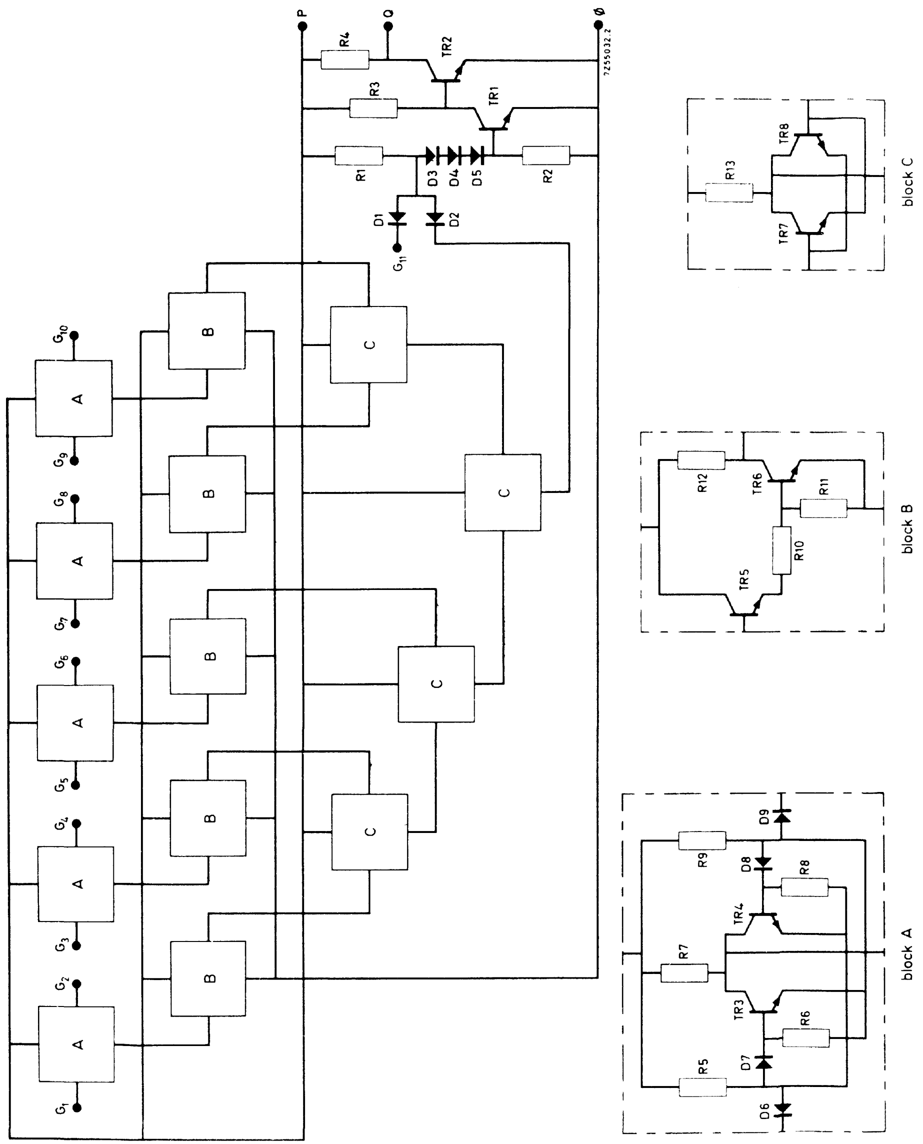


QUICK REFERENCE DATA				
Supply voltage	V_P		6.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C	t_{pd}	typ.	150	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾	7	
D.C. noise margin T_{amb} = 25 °C	M_L	typ.	1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ.	110	mW

The FCH291 comprises nine exclusive-OR functions followed by an AND gate. If an odd number of inputs (G_1 to G_{10}) are HIGH the output will be HIGH, provided G_{11} is HIGH. If an even number of inputs (G_1 to G_{10}) are HIGH the output will be LOW, provided G_{11} is HIGH. If G_{11} is LOW the output will be LOW regardless the condition of other inputs.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLE

G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8	G_9	G_{10}	G_{11}	Q
Even number of inputs HIGH										H	L
Odd number of inputs HIGH										H	H
X	X	X	X	X	X	X	X	X	X	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current	$-I_Q$	max.	20	mA[1]
Input current	$-I_G$	max.	20	mA[2]
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}		-55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

[1] For negative output voltage.
[2] At this limit input voltage typ.: -1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	^{o}C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan-out	N_a	⩾	7	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	0.8	V
Average propagation delay time	t_{pd}	max.	250	ns
Equivalent input capacitance	C_G	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	21	mA
Power dissipation at T_{amb} = +75 ^{o}C	P_{tot}	max.	190	mW

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	see note 1
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	see note 1
		16.0	15.2	14.4	mA	6.3	see note 1
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7 and 6.3	I_Q = 0 (see note 1)
	V_{QHmin}	4.7	4.7	4.5	V	5.7	I_Q = −200 μA
Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input voltage HIGH	V_{GHmin}	3.8	3.8	3.4	V	5.7 and 6.3	
Input current LOW	$-I_{G1\ to\ 10\ Lmax}$	1.75	1.65	1.55	mA	5.7	$V_{G1\ to\ 10}$ = 0.4 V
		2.0	1.9	1.8	mA	6.3	$V_{G1\ to\ 10}$ = 0.4 V
	$-I_{G11max}$	1.9	1.8	1.7	mA	5.7	V_{G11} = 0.4 V
		2.1	2.0	1.9	mA	6.3	V_{G11} = 0.4 V
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Supply current	I_{Pmax}	32.0	30.5	28.0	mA	6.3	G inputs LOW

Note 1

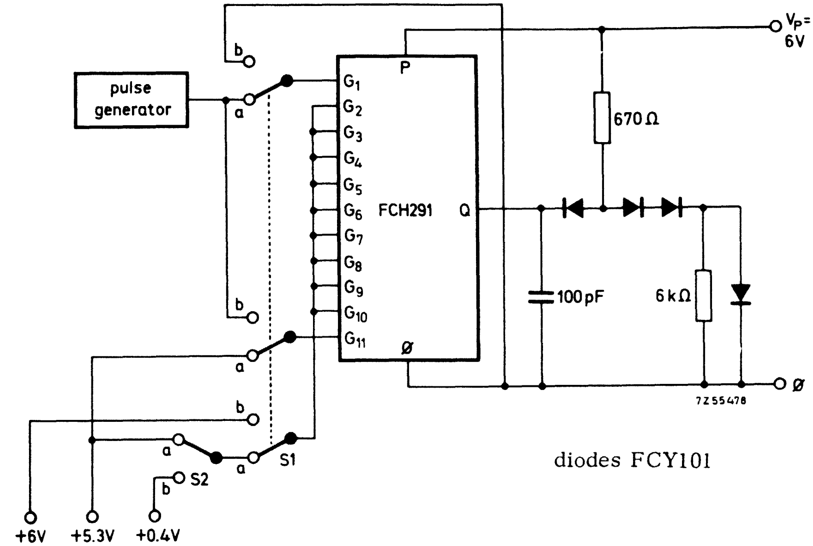
For the proper combination of inputs to be HIGH or LOW see function table on page 2.

CHARACTERISTICS (continued)

		T_{amb} (°C) 0	+25	+75		V_P (V)	Conditions and references	Fig.
DYNAMIC DATA								
Propagation delay times from one G (G_1 to G_{10}) to Q								
Rise propagation delay time	t_{pdrmax}	–	200	–	ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 100 pF all other inputs (including G_{11}) at V_G = 5.3 V	1; 2
Fall propagation delay time	t_{pdfmax}	–	200	–	ns	6.0		
Rise propagation delay time	t_{pdrmax}	–	250	–	ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 100 pF all other inputs (excluding G_{11}) at V_G = 0.4 V V_{G11} = 5.3 V	1; 3
Fall propagation delay time	t_{pdfmax}							
Propagation delay times from G_{11} to Q								
Rise propagation delay time	t_{pdrmax}	–	100	–	ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 100 pF V_{G1} = 0 V all other inputs at V_G = 6.0 V	1; 3
Fall propagation delay time	t_{pdfmax}	–	120	–	ns	6.0		

CHARACTERISTICS (continued)

DYNAMIC DATA



diodes FCY101

Fig. 1 Equivalent load for N = 6; C_L [1]) = 100 pF

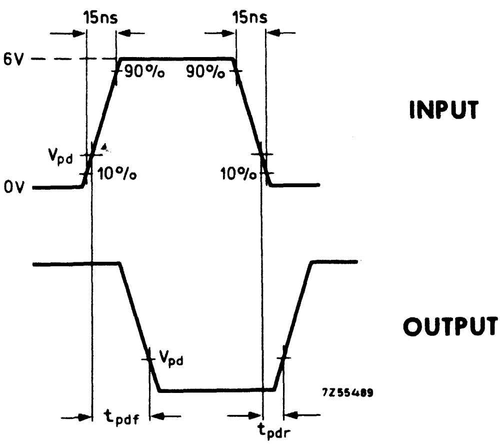


Fig. 2 Switch S2 in position a
Switch S1 in position a

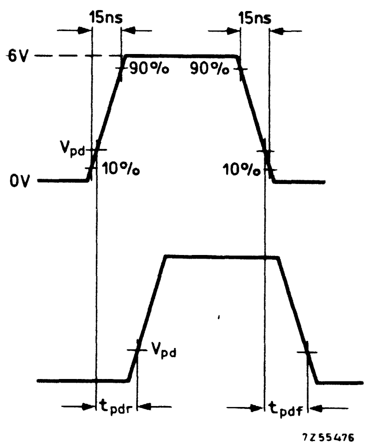


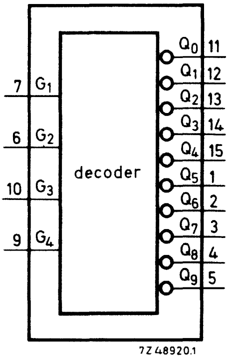
Fig. 3 Switch S1 in position a
Switch S2 in position b
or
Switch S1 in position b
Switch S2 immaterial

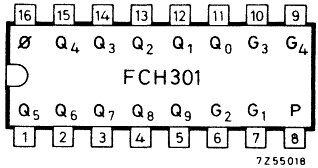
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 4-BIT DECODER



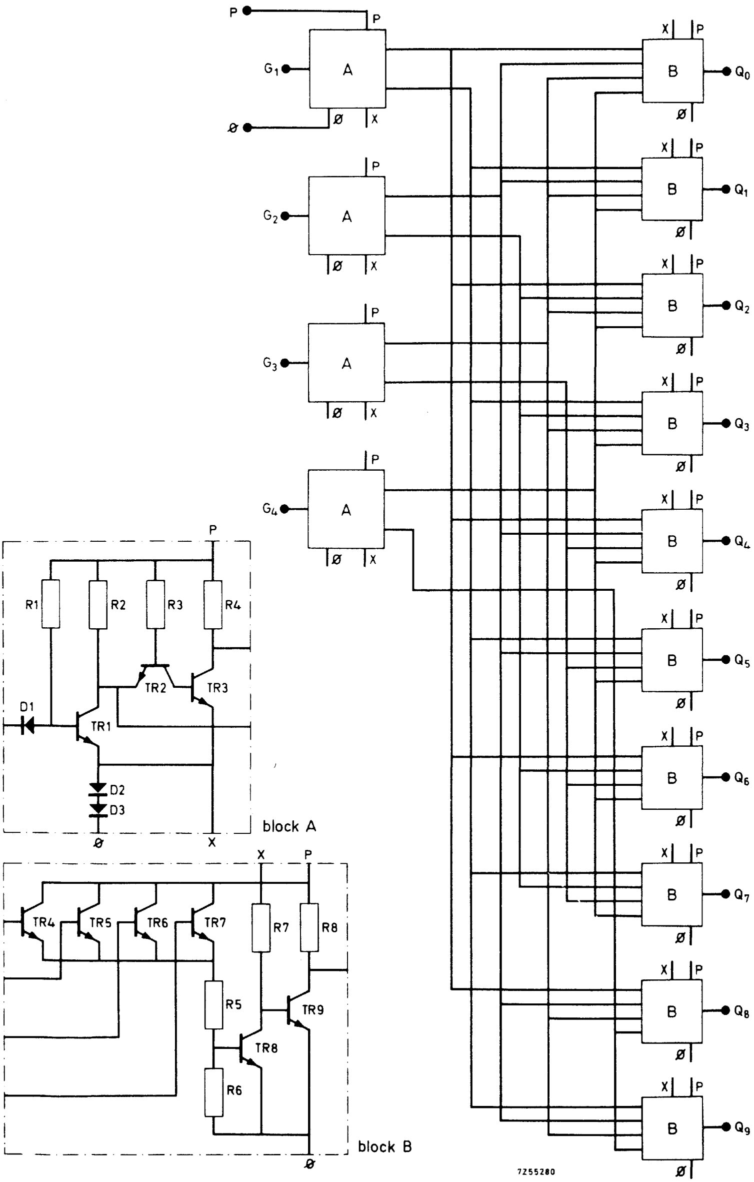


PACKAGE OUTLINE
16 lead plastic dual in-line (type A)
(See General Section)

QUICK REFERENCE DATA			
Supply voltage	V_P	$6.0 \pm 5\%$	V
Operating ambient temperature range	T_{amb}	0 to +75	^oC
Average propagation delay time $N = 1$, $C_W = 40$ pF, $T_{amb} = 25\ ^oC$	t_{pd}	$\leqslant$ 100	ns
Available d.c. fan out $T_{amb} = 0$ to $+75\ ^oC$	N_a	$\geqslant$ 9	
D.C. noise margin $T_{amb} = 25\ ^oC$	M_L	$\geqslant$ 0.6	V
Power consumption 50% duty cycle, $T_{amb} = 25\ ^oC$	P_{av}	typ. 250	mW

The FCH301 is a fast binary (8-4-2-1) to decimal decoder formed by 18 gate functions. All outputs except the decoded one stay HIGH. If the input does not conform to the 8-4-2-1 code, all outputs remain HIGH.

CIRCUIT DIAGRAMS



FUNCTION TABLE

G_4	G_3	G_2	G_1	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

LOGIC FUNCTIONS

$Q_0 = \overline{\overline{G_1} \cdot \overline{G_2} \cdot \overline{G_3} \cdot \overline{G_4}}$

$Q_1 = \overline{G_1 \cdot \overline{G_2} \cdot \overline{G_3} \cdot \overline{G_4}}$

$Q_2 = \overline{\overline{G_1} \cdot G_2 \cdot \overline{G_3} \cdot \overline{G_4}}$

$Q_3 = \overline{G_1 \cdot G_2 \cdot \overline{G_3} \cdot \overline{G_4}}$

$Q_4 = \overline{\overline{G_1} \cdot \overline{G_2} \cdot G_3 \cdot \overline{G_4}}$

$Q_5 = \overline{G_1 \cdot \overline{G_2} \cdot G_3 \cdot \overline{G_4}}$

$Q_6 = \overline{\overline{G_1} \cdot G_2 \cdot G_3 \cdot \overline{G_4}}$

$Q_7 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot \overline{G_4}}$

$Q_8 = \overline{\overline{G_1} \cdot \overline{G_2} \cdot \overline{G_3} \cdot G_4}$

$Q_9 = \overline{G_1 \cdot \overline{G_2} \cdot \overline{G_3} \cdot G_4}$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage at T_{amb}: max. 40 °C	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Input current [1])	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−35 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

1) At this limit, input voltage typ.: −1.5 V.

SYSTEM DESIGN DATA

Operating ambient temperature	T_{amb}	0 to +75	°C
Uniform system voltage	V_P	5.7 to 6.3	V
Available d.c. fan out	N_a	9	
D.C. noise margin	M_L	min. 0.4	V
	M_H	min. 2.9	V
Average propagation delay time	t_{pd}	100	ns
Equivalent input capacitance	C_G	typ. 4	pF
Power dissipation	P_{tot}	max. 300	mW

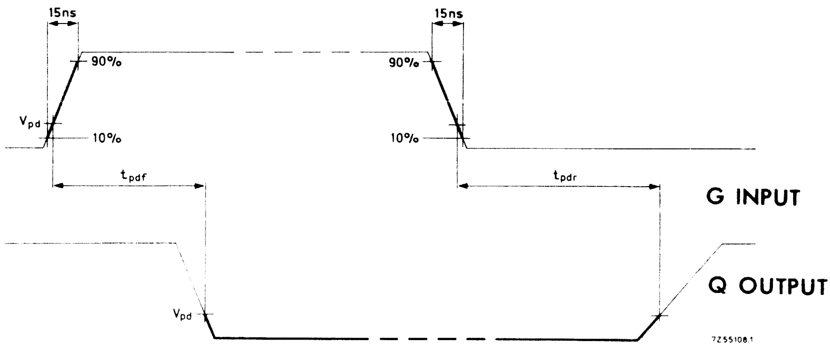
CHARACTERISTICS

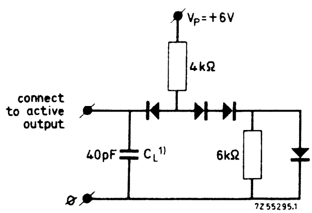
		T_{amb} (°C) 0	25	75		V_P (V)	Conditions and References
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	For the proper combination of inputs to be HIGH or LOW see Function Table
at: Output current LOW	I_{QLmax}	15.8	14.9	14.0	mA	5.7	
	I_{QLmax}	18.0	17.1	16.2	mA	6.3	
Output voltage HIGH	V_{QHmin}	5.2	5.2	5.2	V	5.7	$-I_Q = 0$
Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input voltage HIGH	V_{GHmin}	2.6	2.5	2.4	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75	1.65	1.55	mA	5.7	V_G = 0.4 V
	$-I_{GLmax}$	2.0	1.9	1.8	mA	6.3	V_G = 0.4 V
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA		V_G = 6.3 V other inputs 0 V
Supply current	I_{Pmax}	–	–	48	mA	6.3	G inputs 0 V

CHARACTERISTICS (continued)

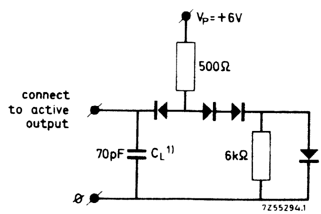
		T_{amb} (°C) 0	25	75		Conditions and References V_P (V)	
DYNAMIC DATA*)							
Rise propagation delay time	t_{pdr} max	–	110	–	ns		V_{pd} = 1.5 V; N = 1; C_L = 40 pF
	t_{pdr} max	–	80	–	ns		V_{pd} = 1.5 V; N = 8; C_L = 70 pF
Fall propagation delay time	t_{pdf} max	–	85	–	ns		V_{pd} = 1.5 V; N = 1; C_L = 40 pF
	t_{pdf} max	–	100	–	ns		V_{pd} = 1.5 V; N = 8; C_L = 70 pF

*) See figures below





N = 1



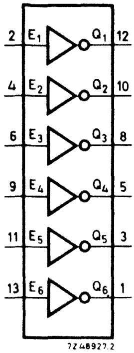
N = 8

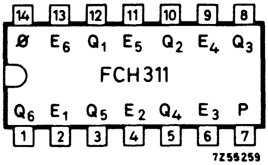
diodes FCY101

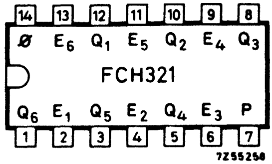
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}
1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SEXTUPLE INVERTER







	non-R_C	R_C
Sextuple inverter	FCH311	FCH321

QUICK REFERENCE DATA

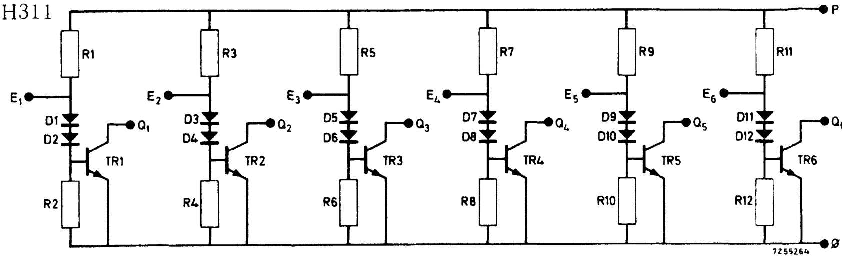
Supply voltage	V_P	6.0 ± 5%		V
Operating ambient temperature range	T_{amb}	0 to +75		^oC
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 ^oC	t_{pd}	typ.	30	ns
Available d.c. fan out to FC gates T_{amb} = 0 to +75 ^oC	N_a	≥	8	
Power consumption per inverter 50% duty cycle, T_{amb} = 25 ^oC non-R_C	P_{av}	typ.	7	mW
R_C	P_{av}	typ.	11	mW

The fan-in of the circuits can easily be expanded by means of a diode array.
The outputs of these inverters may be interconnected to perform the AND-OR-NOT function.

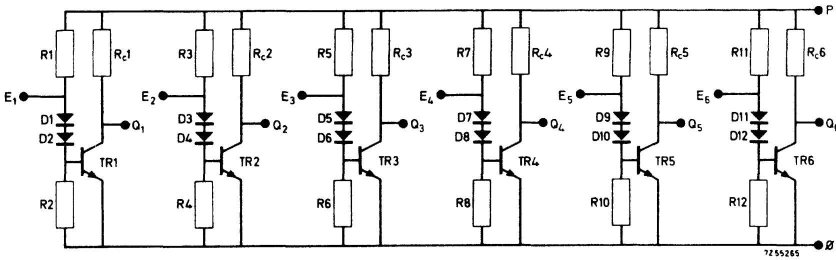
PACKAGE OUTLINES: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAMS

FCH311

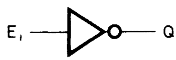


FCH321



LOGIC FUNCTION

1. Individual inverter operation

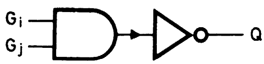


Function table

E_i	Q
L	H
H	L

$Q = \overline{E_i}$ for positive logic

2. Individual gate operation



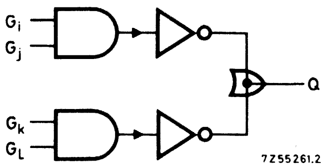
Function table

G_i	G_j	Q
L	X	H
X	L	H
H	H	L

$Q = \overline{G_i \cdot G_j}$ for positive logic

LOGIC FUNCTION (continued)

3. Commoned gate operation



Function table

G_i	G_j	G_k	G_l	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

$Q = (\overline{G_i . G_j}) . (\overline{G_k . G_l}) = \overline{(G_i . G_j) + (G_k . G_l)}$ for positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

The AND-function is obtained by connecting a **diode array to the E input.**

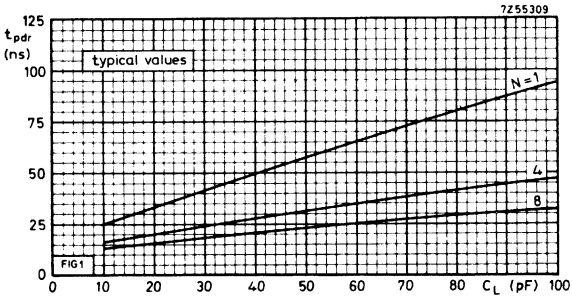
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage (HIGH state)	V_Q	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Expander input voltages with respect to supply	V_P-V_E	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

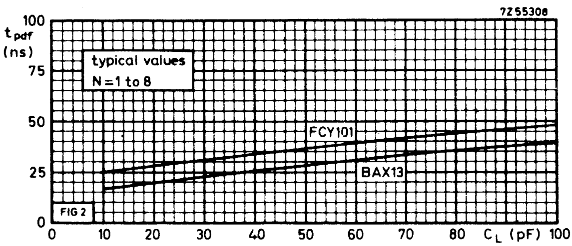
[1]) For negative output voltage.

SYSTEM DESIGN DATA (both non-R_c and R_c)

Uniform system temperature		T_{amb}		0 to +75	^{o}C
Uniform system supply voltage		V_p		5.7 to 6.3	V
Available d.c. fan out to FC gates		N_a	≥	8	
Averaged propagation delay time with BAX13 diode		t_{pd}	max.	75	ns
Increase of t_{pdf} with increasing expander capacitance for C_W = 0 to 100 pF		Δt_{pdf}	typ.	1.4	ns/pF
Equivalent output capacitance		C_Q	typ.	10	pF
Supply current (duty cycle 50%)	non-R_c	I_{Pav}	typ.	7.2	mA
	R_c	I_{Pav}	typ.	10.5	mA
Power dissipation at T_{amb} = 75 ^{o}C	non-R_c	P_{tot}	max.	100	mW
	R_c	P_{tot}	max.	171	mW



t_{pdr} versus C_L for both BAX13 and FCY101 as input diode



t_{pdf} versus C_L for BAX13 and FCY101 as input diode

CHARACTERISTICS of FCH311 (non R_c)

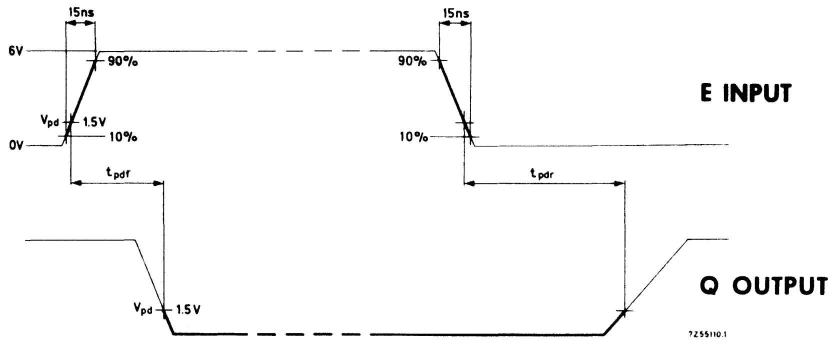
		T_{amb} (°C) 0	+25	+75		V_P (V)	Conditions and references
STATIC DATA Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	$-I_E$ = 50 μA
at: Output current LOW	I_{QLmax}	16.0 18.0	15.1 17.0	14.2 16.0	mA mA	5.7 6.3	
Expander input voltage HIGH	V_{EHmax}	3.0	2.8	2.6	V	5.7 and 6.3	I_{QL} = I_{QL} max $-I_E$ = 50 μA
Input current LOW	$-I_{ELmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	
at: Expander input voltage LOW	V_{EL}	1.05	1.00	0.90	V		
Output current HIGH	I_{QHmax}	70	70	70	μA	5.7 and 6.3	V_Q = 5.3 V
at: Expander input voltage LOW	V_{ELmax}	1.8	1.7	1.4	V	5.7 and 6.3	
Supply current	I_{PHmax}	12.0	11.4	10.8	mA	6.3	
at: Expander input voltage LOW	V_{EL}	1.05	1.00	0.90	V		
Supply current	I_{PLmax}	11.4	10.2	10.2	mA	6.3	Expander inputs floating
DYNAMIC DATA see also page 7	t_{pdr} max	-	85	-	ns	6.0	R = 4 kΩ C_L = 40 pF
Rise propagation delay time	t_{pdr} max	-	70	-	ns	6.0	R = 670 Ω C_L = 60 pF
	t_{pdf} max	-	65	-	ns	6.0	R = 4 kΩ C_L = 40 pF
Fall propagation delay time	t_{pdf} max	-	85	-	ns	6.0	R = 670 Ω C_L = 60 pF

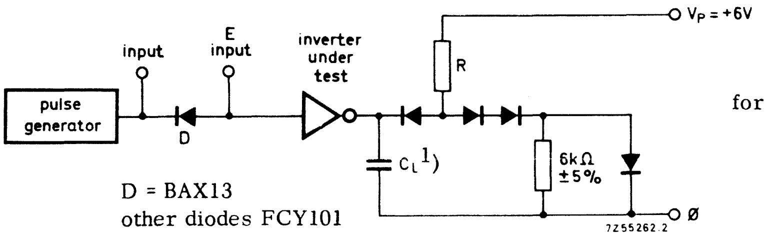
CHARACTERISTICS of FCH321 (R_c)

		T_{amb} (°C) 0	+25	+75		V_P (V)	Conditions and references
STATIC DATA Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	$-I_E$ = 50 μA
at: Output current LOW	I_{QLmax}	14.0 16.0	13.2 15.2	12.4 14.4	mA mA	5.7 6.3	
Expander input voltage HIGH	V_{EHmax}	3.0	2.8	2.6	V	5.7 and 6.3	I_{QL} = I_{QL} max $-I_E$ = 50 μA
Output voltage HIGH	V_{QHmin}	5.3 4.1	5.3 4.1	5.3 3.9	V V	5.7 5.7	I_Q = 0 I_Q = −200 μA
at: Expander input voltage LOW	V_{ELmax}	1.8	1.7	1.4	V	5.7 and 6.3	
Input current LOW	$-I_{ELmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	
at: Expander input voltage LOW	V_{EL}	1.05	1.00	0.90	V		
Output current LOW (AND-OR-NOT function)	$-I_{QLLmax}$	2.2	2.1	2.0	mA	6.3	Expander inputs LOW Output forced LOW externally to V_Q = 0.4 V
Supply current	I_{PLmax}	25.2	22.8	21.6	mA	6.3	Expander inputs floating
DYNAMIC DATA see also page 7 Rise propagation delay time	t_{pdr} max	–	85	–	ns	6.0	R = 4 kΩ C_L = 40 pF
	t_{pdr} max	–	70	–	ns	6.0	R = 670 Ω C_L = 60 pF
Fall propagation delay time	t_{pdf} max	–	65	–	ns	6.0	R = 4 kΩ C_L = 40 pF
	t_{pdf} max	–	85	–	ns	6.0	R = 670 Ω C_L = 60 pF

CHARACTERISTICS (continued)

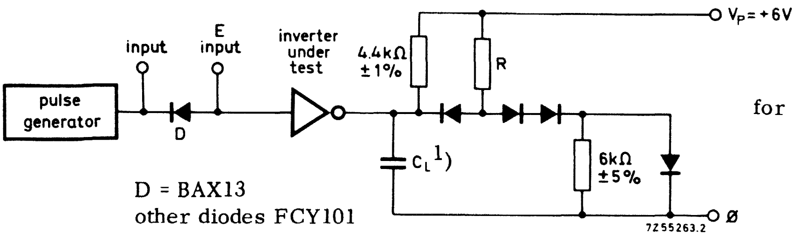
DYNAMIC DATA





for FCH321

D = BAX13
other diodes FCY101



for FCH311

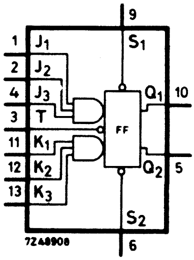
D = BAX13
other diodes FCY101

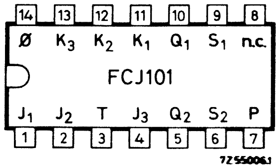
Waveforms and loading circuits, illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK FLIP-FLOP



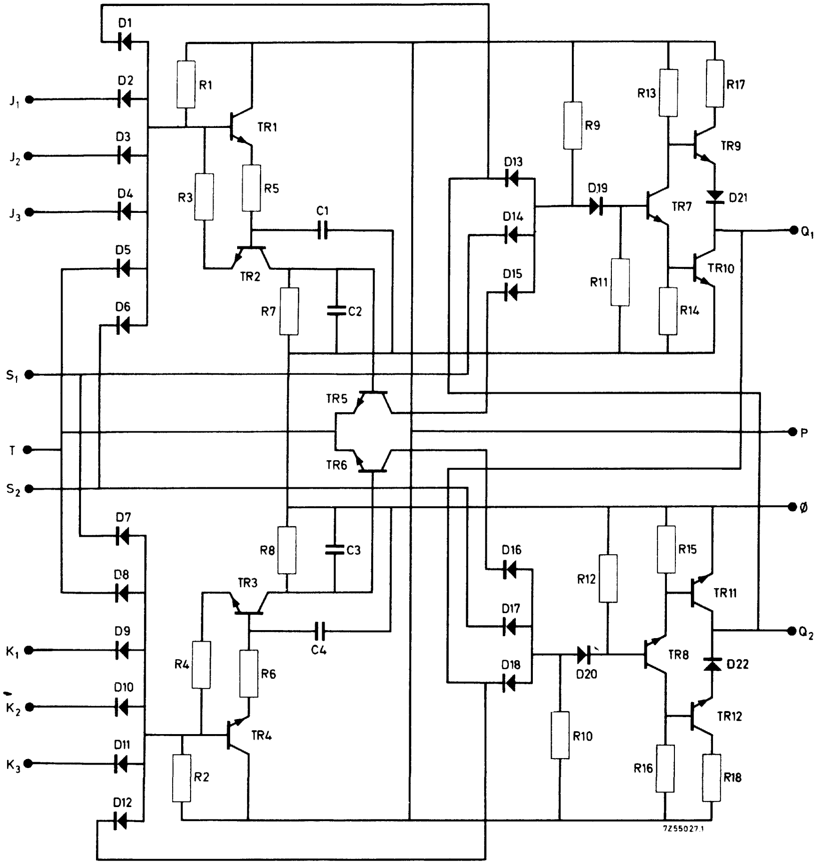


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 10	MHz
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	≥ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 36	mW

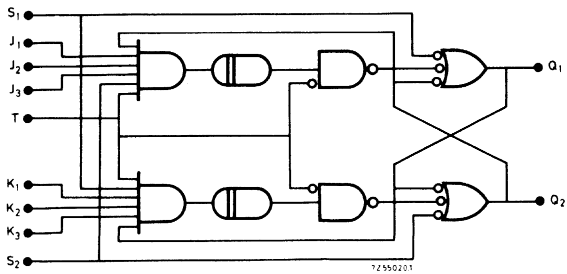
The FCJ101 performs the JK flip-flop operation. Three J and three K inputs permit an additional AND operation. Triggering occurs at the falling edge of a T signal. The direct-set inputs (overriding any other inputs) are active at the LOW level. The circuitry incorporates bi-directional outputs for driving capacitive loads. Typical applications are in high speed counters and shift registers.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal

T = HIGH		T = LOW	
J	K	Q_1	Q_2
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the flip-flop by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1 and S_2 should be HIGH or floating.

$J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$
} for positive logic

2. Set or reset via S terminals

S_1	S_2	Q_1	Q_2
H	L	L	H
L	H	H	L
L	L	H	H
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS (Limiting values) [1])

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2])	$-I_Q$	max.	20	mA
Input current [3])	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

[1]) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
[2]) For negative output voltage in LOW state.
[3]) At this limit input voltage typ. : −1.5V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to J or K input	$N_{aJ} = N_{aK}$	⩾	8	
to S input	N_{aS}	⩾	4	
to G input	N_{aG}	⩾	8	
Available a.c. fan out to T input	N_{aT}	⩾	2	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	0.2	V
to J or K input	M_L	min.	0.5	V
	M_H	min.	0.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	0.2	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	85	ns
Maximum clock rate	f_c	⩾	6	MHz
Equivalent input capacitances				
for T input	C_T	typ.	30	pF
for J or K input	$C_J = C_K$	typ.	20	pF
for S input	C_S	typ.	25	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	6.0	mA
Power dissipation at $T_{amb} = 75\ ^oC$	P_{tot}	max.	56	mW

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	16.5	12.4	mA	5.7	
		16.0	19.0	14.4	mA	6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	$I_Q = -100\ \mu A$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.75	1.65	1.55	mA	5.7	$V_J = V_K = 0.4$ V; other inputs floating
		2.0	1.9	1.8	mA	6.3	
	$-I_{TLmax}$	3.5	3.3	3.1	mA	5.7	$V_T = 0.4$ V; other inputs floating
		4.0	3.8	3.6	mA	6.3	
	$-I_{SLmax}$	3.5	3.3	3.1	mA	5.7	$V_S = 0.4$ V; other inputs floating
		4.0	3.8	3.6	mA	6.3	
Input current HIGH	$-I_{JHmax}$, $-I_{KHmax}$	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	2	2	50	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	9	–	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		V_P (V)	Conditions and references	fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH	V_{THmin} V_{JHmin} V_{KHmin}	3.6	3.3	3.0	V		HIGH level at T and J and/or K to be present simultaneously	1
during: Input time HIGH	t_{THmin}	50	50	50	ns			1
followed by: T-input slope	$(-\frac{dt}{dV})_{Tmax}$	18	18	18	ns/V			1
	$(-\frac{dt}{dV})_{Tmin}$	4	4	4	ns/V			1
to: T-input voltage LOW	V_{TLmax}	0.7	0.7	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
JK-input voltage LOW	V_{JLmax} V_{KLmax}	1.1	1.0	0 9	V		J and K turning LOW after T and J and/or K having been HIGH simultaneously	2
during: JK-input time LOW	t_{JLmin} t_{KLmin}	100	100	160	ns			2
Clock skew protection								
Hold time LOW	$t_{holdLmax}$	15	15	15	ns			2
Hold time HIGH	$t_{holdHmax}$	7	10	10	ns			3
Set or Reset								
S-input voltage LOW	V_{SLmax}	1.0	0.9	0.7	V		active $t_{SLmin} = t_{pdf}$	4
S-input voltage HIGH	V_{SHmin}	3.6	3.3	3.0	V		inactive	
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	70	–	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 60 pF	5
Fall propagation delay time	$t_{pdf\,max}$	–	100	–	ns	6.0	V_{pd} = 1.5 V N = 8; C_L = 60 pF other output N = 1 C_L = 60 pF	5

CHARACTERISTICS (continued)

DYNAMIC DATA

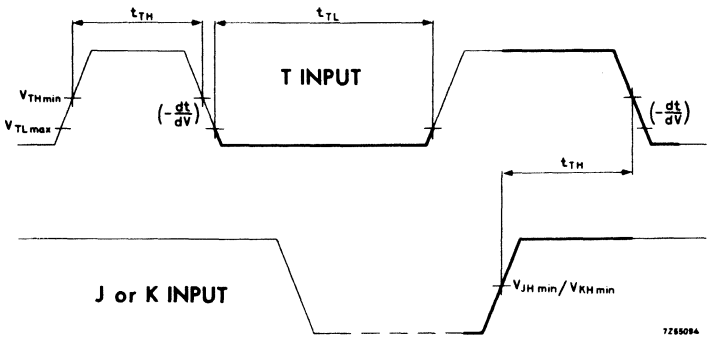


Fig.1. Waveforms illustrating conditions for change of state.

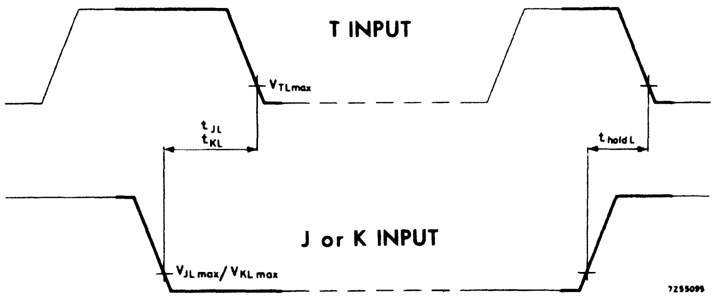


Fig.2. Waveforms illustrating conditions for no change of state.

For no change of state to result:

a. the time between J or K reaching V_{JLmax}, V_{KLmax} (going LOW) and T reaching V_{TLmax} (going LOW) must be at least t_{JLmin}, t_{KLmin}.

b. the time between J or K reaching V_{JLmax}, V_{KLmax} (going HIGH) and T reaching V_{TLmax} (going LOW) must be less than t_{holdL}.

CHARACTERISTICS (continued)

DYNAMIC DATA

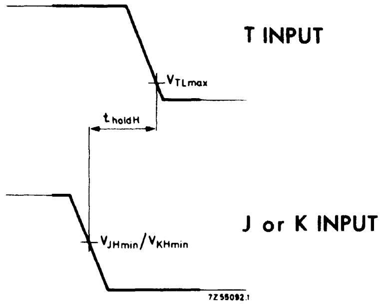


Fig.3. Waveforms illustrating conditions for change of state.
For a change of state still to result, the time between J or K reaching V_{JHmin}, V_{KHmin} (going LOW) and T reaching V_{TLmax} (going LOW) must be less than t_{holdH}

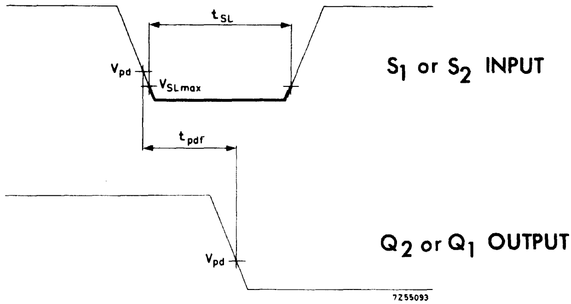
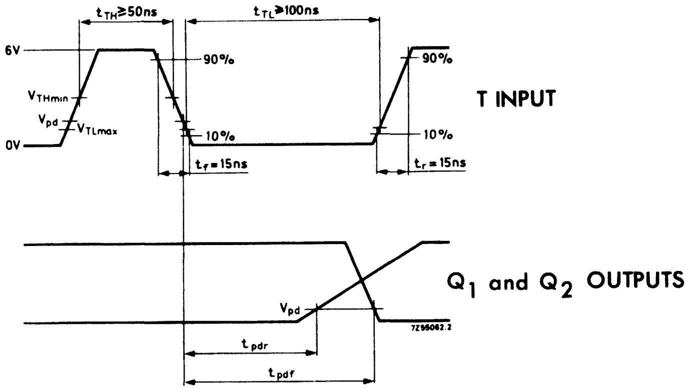
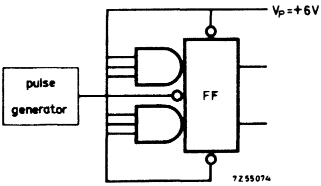


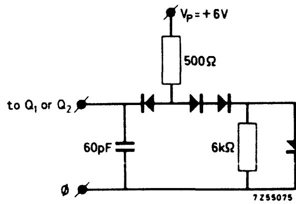
Fig.4. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

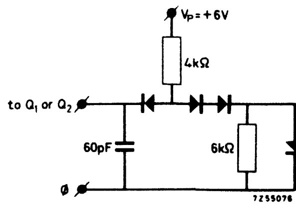






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 60 pF



diodes FCY101

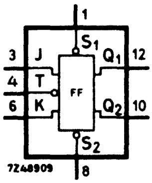
Equivalent load for N = 1 and C_L[1]) = 60 pF

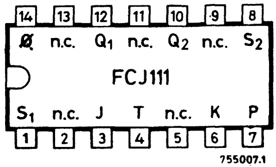
Fig. 5. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK MASTER-SLAVE FLIP-FLOP



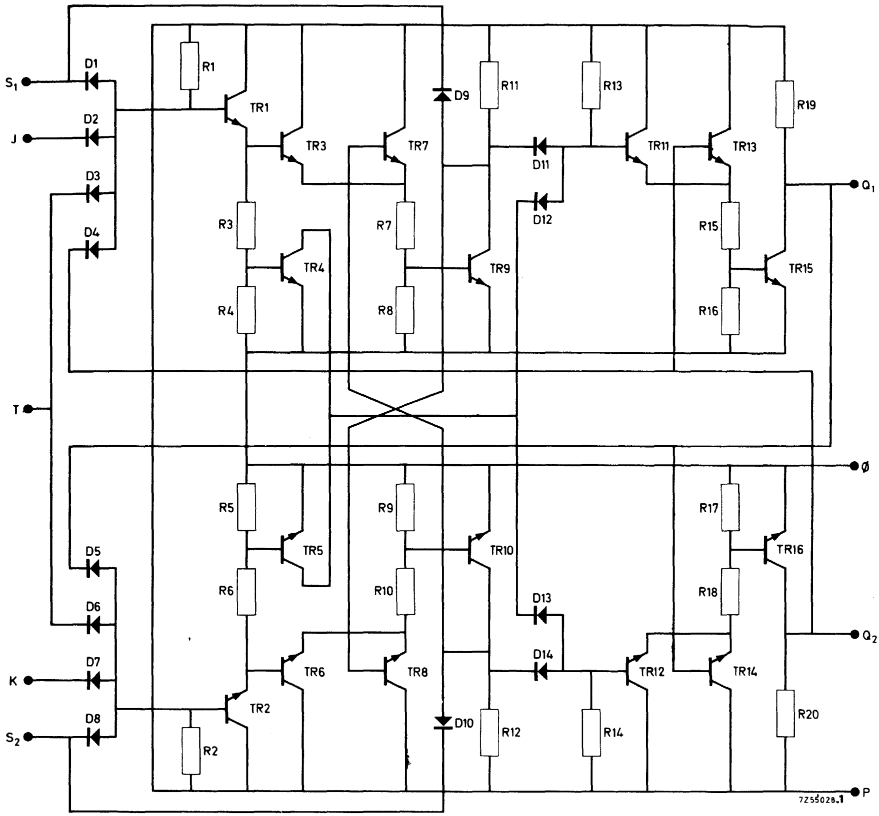


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 5	MHz
Available d.c. fan-out T_{amb} = 0 to 75 °C	N_a	≥ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 67	mW

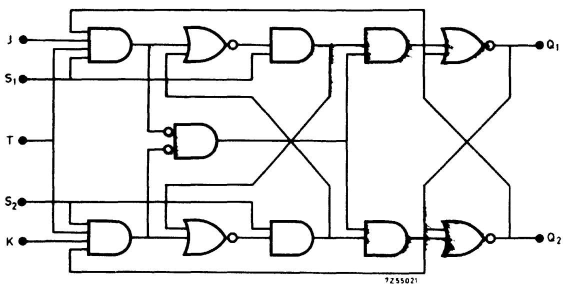
The FCJ111 is a direct-coupled JK flip-flop, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signal, are immaterial. The J, K and T inputs are logically equivalent, allowing the use of J and K for triggering. The direct set-inputs (overriding any other inputs) are active at the LOW level.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM(to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J	K	Q_1	Q_2
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1 or S_2 should be HIGH or floating.

2. Trigger action via J and K terminals

J	K	Q_1	Q_2
H→L	X	H	L
X	H→L	L	H
H→L	H→L	reversed	

If J or K go LOW with T HIGH, Q_1 and Q_2 assume the state shown. If both J and K go LOW with T HIGH, the outputs of Q_1 and Q_2 are reversed (exactly as if J and K remained HIGH and T were triggered). When triggering on J and K the T input requirements V_{TH} and V_{TL} (see CHARACTERISTICS) apply to J and K.
S_1 and S_2 should be HIGH or floating.

3. Set or reset via S terminals

S_1	S_2	Q_1	Q_2
H	L	L	H
L	H	H	L
L	L	indeterminate	
H	H	no change	

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

The set inputs override the other inputs and directly determine the outputs of the flip-flop.
In the case of both set inputs going LOW the first to reach LOW will determine the output conditions.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

[1] For negative output voltage.
[2] At this limit input voltage typ.: −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	^{o}C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to T input	N_{aT}	⩾	4	
to J or K input	$N_{aJ} = N_{aK}$	⩾	8	
to S input	N_{aS}	⩾	5	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.5	V
	M_H	min.	1.9	V
to J or K input	M_L	min.	0.9	V
	M_H	min.	1.9	V
to S input	M_L	min.	0.4	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	2.3	V
Average propagation delay time	t_{pd}	max.	150	ns
Maximum clock rate	f_c	⩾	3	MHz
Equivalent input capacitances				
for T input	C_T	typ.	8	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	8	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	11.2	mA
Power dissipation at $T_{amb} = 75\ ^{o}C$	P_{tot}	max.	110	mW

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	
		16.0	15.2	14.4	mA	6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.4	5.3	V	5.7	$I_Q = 0$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.9	3.5	2.8	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	350	450	550	µA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.75	1.65	1.55	mA	5.7	$V_J = V_K = 0.4$ V; other inputs floating
		2.0	1.9	1.8	mA	6.3	
	$-I_{TLmax}$	3.5	3.3	3.1	mA	5.7	$V_T = 0.4$ V; other inputs floating
		4.0	3.8	3.6	mA	6.3	
	$-I_{SLmax}$	2.7	2.6	2.4	mA	5.7	$V_S = 0.4$ V; other inputs floating
		3.0	2.9	2.7	mA	6.3	
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	µA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	2	2	50	µA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	µA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	20	–	mA	6.3	J, K, S,T inputs HIGH

CHARACTERISTICS

		T_{amb} (°C) 0 +25 +75	Conditions and references: V_P (V)		fig.
DYNAMIC DATA			5.7 and 6.3		
Change of state					
Input voltage HIGH	V_{THmin} V_{JHmin} V_{KHmin}	3.1 2.9 2.5 V		HIGH level at T and J and/or K to be present simultaneously	1
during: T-input time HIGH	t_{THmin}	100 100 100 ns			1
to: Input voltage LOW	V_{TLmax}	1.3 1.1 0.9 V		$t_{TLmin} = t_{pdr}$	1
No change of state					
JK input voltage LOW	V_{JLmax} V_{KLmax}	1.8 1.6 1.3 V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection					
Hold time	$t_{holdmax}$	20 20 20 ns			2
Set or Reset					
S input voltage LOW	V_{SLmax}	1.2 1.0 0.8 V		active $t_{SLmin} = t_{pdr}$	3
S input voltage HIGH	V_{SHmin}	3.1 2.9 2.5 V		inactive	
DYNAMIC DATA					
Propagation delay times from T to Q					
Rise propagation delay time	$t_{pdr\,max}$	- 200 - ns		$V_{pd} = 1.5$ V; N = 1; $C_L = 60$ pF; other output N = 8; $C_L = 56$ pF	4
Fall propagation delay time	$t_{pdf\,max}$	- 100 - ns		$V_{pd} = 1.5$ V; N = 8; $C_L = 56$ pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

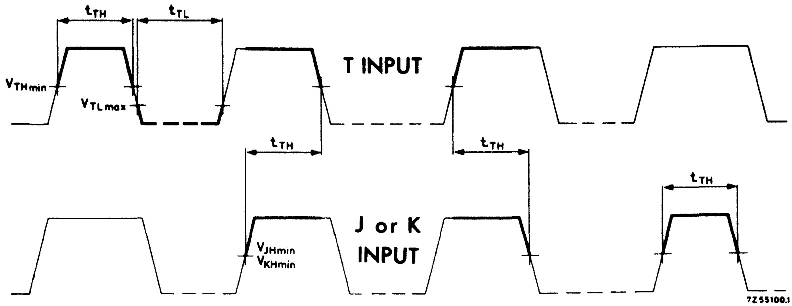


Fig. 1. Waveforms illustrating conditions for change of state.

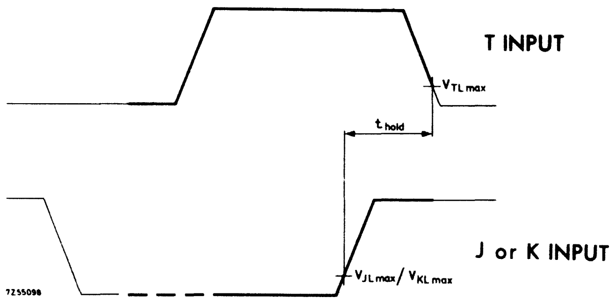


Fig. 2. Waveforms illustrating conditions for no change of state.

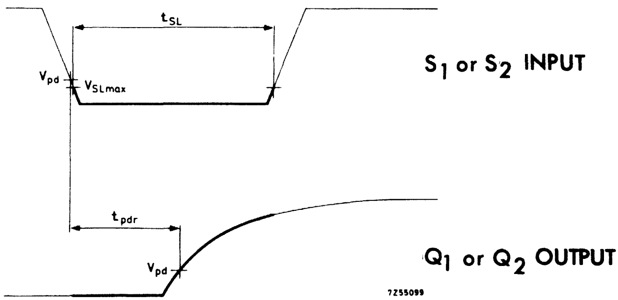
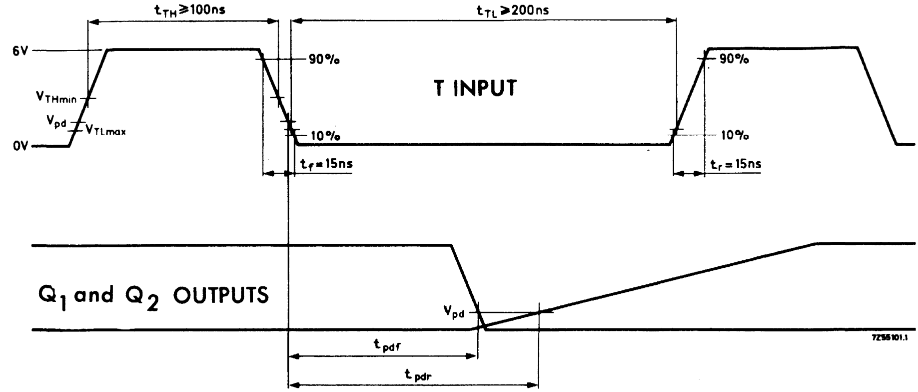
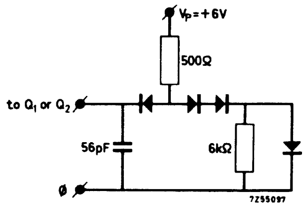


Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

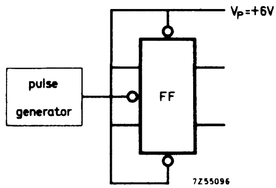
DYNAMIC DATA

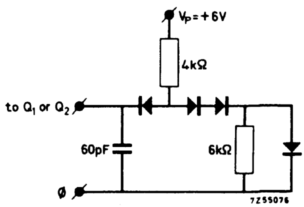




diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 56 pF





diodes FCY101

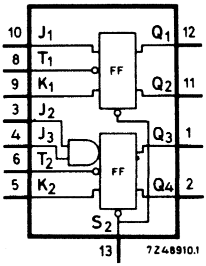
Equivalent load for N = 1 and C_L[1]) = 60 pF

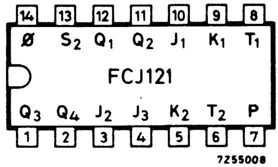
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP-FLOP



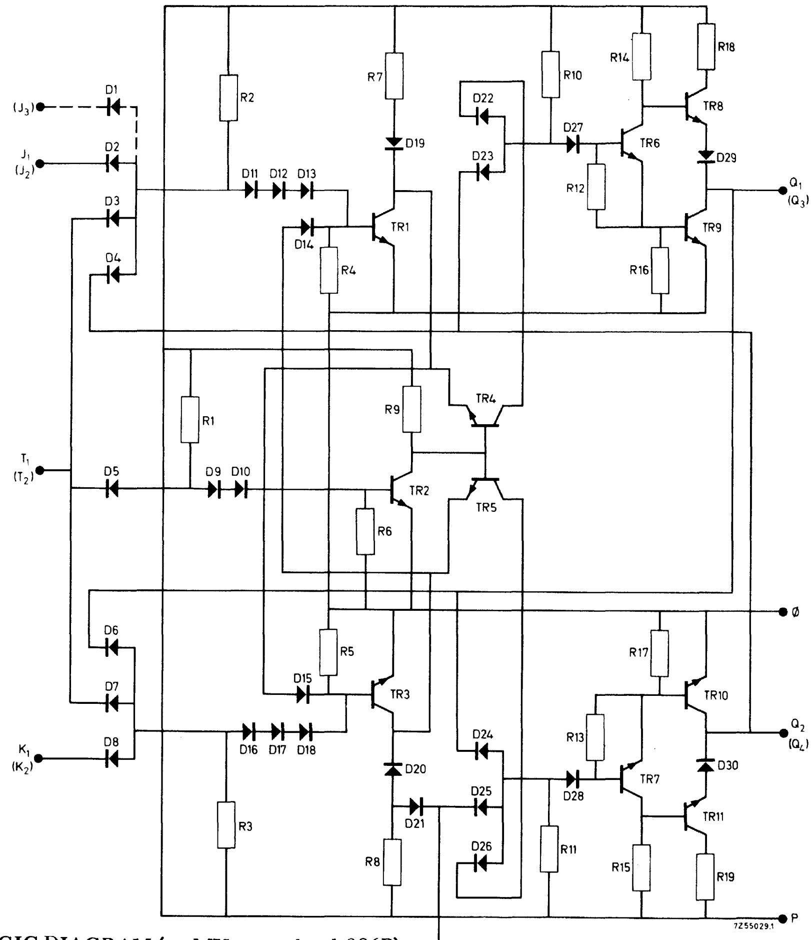


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	≥ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C (each flip-flop)	P_{av}	typ. 50	mW

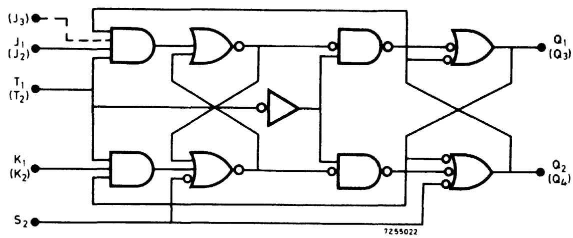
The FCJ121 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals including trigger signals are immaterial. The common set-input (overriding any other inputs) is active at the LOW level. Typical applications are in medium speed counters.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 J_2	K_1 K_2	Q_1 Q_3	Q_2 Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Input S_2 should be HIGH or floating.

For the flip-flop with two J-inputs: $J = J_2 \cdot J_3$ for positive logic

2. Set or Reset via S_2 terminal (both flip-flops)

S_2 S_4	Q_1 Q_3	Q_2 Q_4
L	L	H
H	no change	

The set input overrides the other inputs and directly determines the outputs of both flip-flops.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}		-55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

[1]) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

[2]) For negative output voltage in LOW state.

[3]) At this limit input voltage typ. : −1.5 V

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to T input	N_{aT}	≥	3	
to J or K input	$N_{aJ} = N_{aK}$	≥	10	
to S input	N_{aS}	≥	2	
to G input	N_{aG}	≥	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	≥	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	12	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	16	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1] Both flip-flops together.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QL}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	16.5	12.4	mA	5.7	
		16.0	19.0	14.4	mA	6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	I_Q = −100 μA
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4	1.3	1.2	mA	5.7	V_J = V_K = 0.4 V; other inputs floating
		1.6	1.5	1.4	mA	6.3	
	$-I_{TLmax}$	4.0	3.8	3.5	mA	5.7	V_T = 0.4 V; other inputs floating
		4.5	4.2	3.9	mA	6.3	
	$-I_{SLmax}$	5.7	5.5	5.2	mA	5.7	V_S = 0.4 V; other inputs floating
		6.6	6.3	5.8	mA	6.3	
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	V_J = V_K = 5.3 V other inputs 0 V
	I_{THmax}	3	3	75	μA	5.7	V_T = 5.3 V other inputs 0 V
	I_{SHmax}	4	4	100	μA	5.7	V_S = 5.3 V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	–	26.7	–	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		V_P (V)	Conditions and references	fig.
<u>DYNAMIC DATA</u>						5.7 and 6.3		
<u>Change of state</u>								
Input voltage HIGH	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
during: Input time HIGH	t_{THmin}	60	60	60	ns			1
to: T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
<u>No change of state</u>								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
<u>Clock skew protection</u>								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
<u>Reset</u>								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
<u>DYNAMIC DATA</u>								
<u>Propagation delay times from T to Q</u>								
Rise propagation delay time	$t_{pdr\,max}$	-	90	-	ns	6.0	V_{pd} = 1.5 V; N = 1; C_L = 60 pF	4
Fall propagation delay time	$t_{pdf\,max}$	-	120	-	ns	6.0	V_{pd} = 1.5; N = 8; C_L = 60 pF; other output: N = 1; C_L = 60 pF	4

CHARACTERISTICS(continued)

DYNAMIC DATA

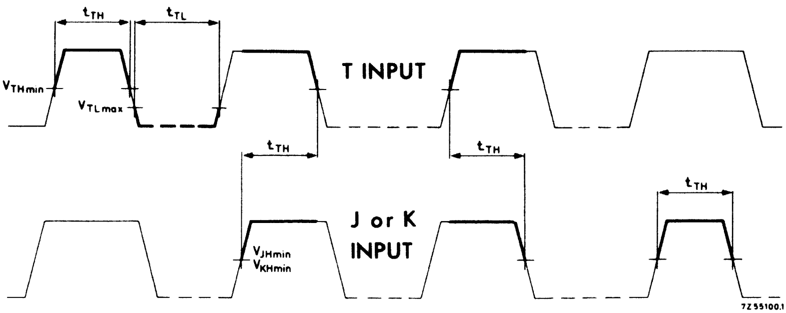


Fig. 1. Waveforms illustrating conditions for change of state.

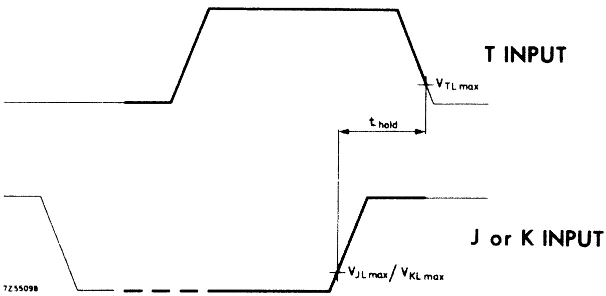


Fig. 2. Waveforms illustrating conditions for no change of state.

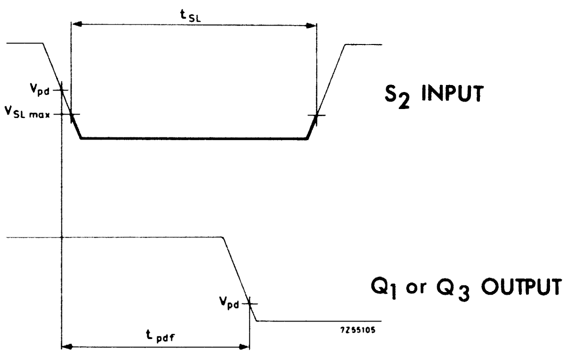
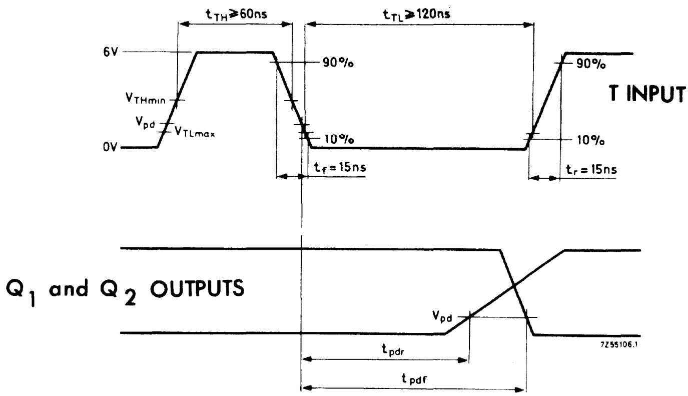
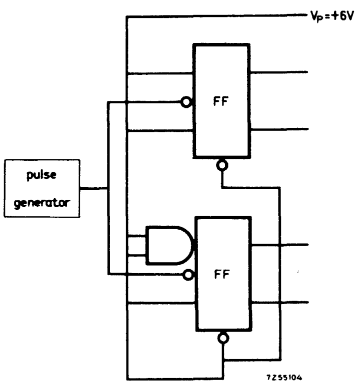


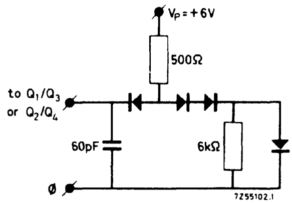
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

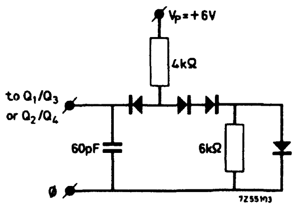






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 60 pF



diodes FCY101

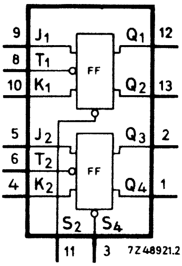
Equivalent load for N = 1 and C_L[1]) = 60 pF

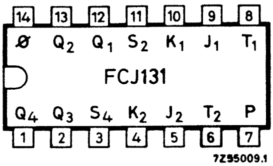
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP FLOP



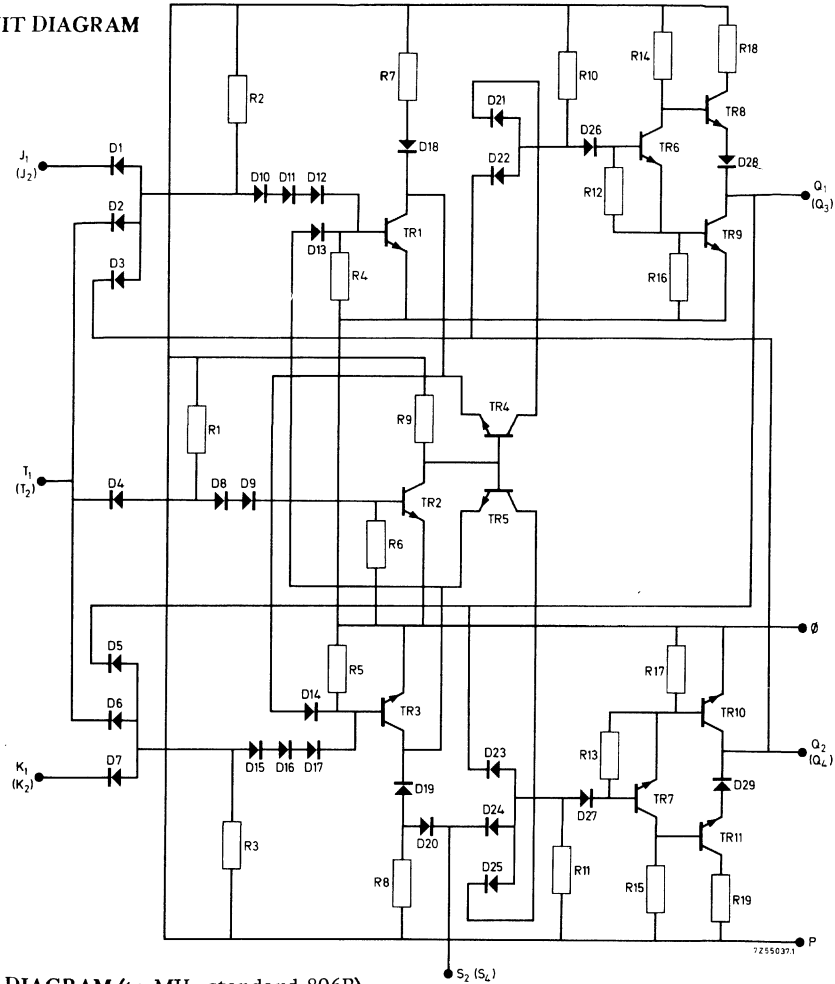


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan out T_{amb} = 25 °C	N_a	≥ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 100	mW

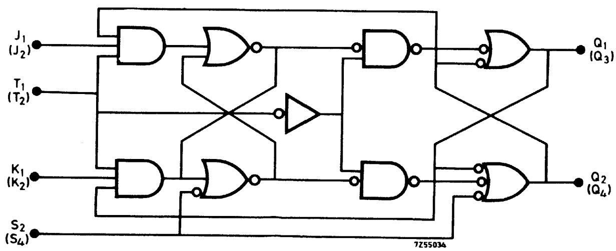
The FCJ131 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signals, are immaterial. The separate set inputs (overriding any other inputs) are active at the LOW level. Typical applications include counters and shift registers.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 / J_2	K_1 / K_2	Q_1 / Q_3	Q_2 / Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_2 and S_4 should be HIGH or floating.

2. Set or reset via S terminals (each flip-flop)

S_2 / S_4	Q_1 / Q_3	Q_2 / Q_4
L	L	H
H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

[1]) For negative output voltage in LOW state.
[2]) At this limit input voltages typ. : −1.5V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to T input	N_{aT}	⩾	3	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS}	⩾	4	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	12	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	8	pF
Supply current (duty cycle 50%) [1])	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1])	P_{tot}	max.	150	mW

[1]) Both flip-flops together

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		V_P (V)	Conditions and references
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	16.5	12.4	mA	5.7	
		16.0	19.0	14.4	mA	6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	I_Q = −100 μA
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4	1.3	1.2	mA	5.7	$V_J = V_K = 0.4$ V; other inputs floating
		1.6	1.5	1.4	mA	6.3	
	$-I_{TLmax}$	4.0	3.8	3.5	mA	5.7	$V_T = 0.4$ V; other inputs floating
		4.5	4.2	3.9	mA	6.3	
	$-I_{SLmax}$	2.9	2.8	2.6	mA	5.7	$V_S = 0.4$ V; other inputs floating
		3.3	3.2	2.9	mA	6.3	
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	3	3	75	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	-	26.7	-	mA	6.3	T inputs LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
during: Input time HIGH	t_{THmin}	60	60	60	ns			1
to: T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	-	90	-	ns	6.0	V_{pd} = 1.5 V; N = 1; C_L = 60 pF	4
Fall propagation delay time	$t_{pdf\,max}$	-	120	-	ns	6.0	V_{pd} = 1.5; N = 8; C_L = 60 pF; other output: N = 1; C_L = 60 pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

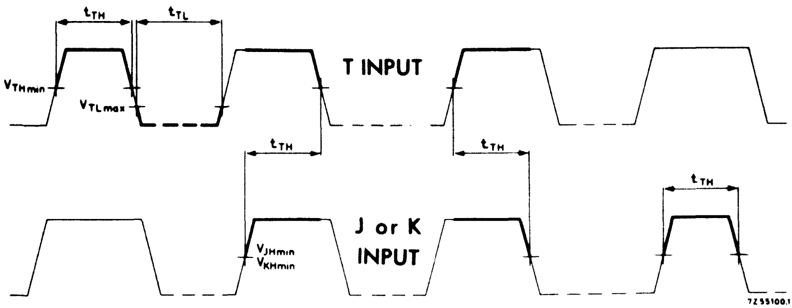


Fig. 1. Waveforms illustrating conditions for change of state.

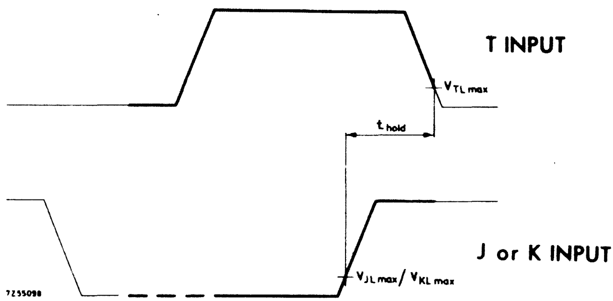


Fig. 2. Waveforms illustrating conditions for no change of state.

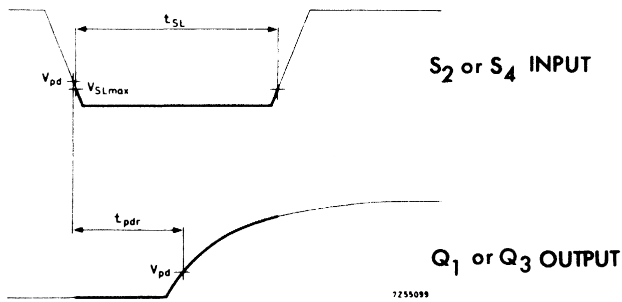
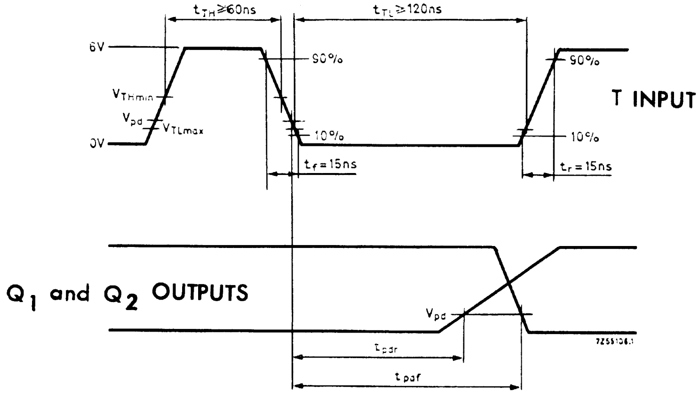
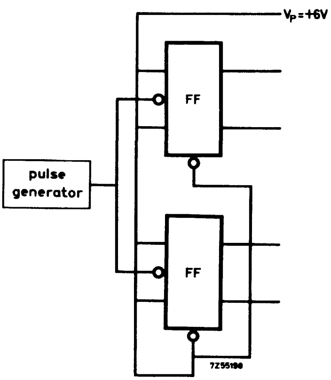


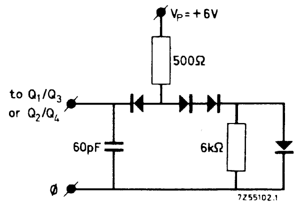
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

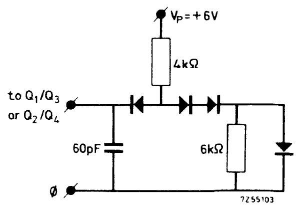
DYNAMIC DATA







Diodes FCY101
Equivalent load for N = 8 and
C_L 1) = 60 pF



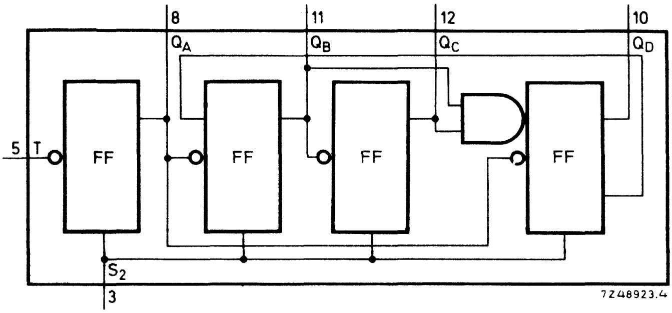
Diodes FCY101
Equivalent load for N = 1 and
C_L 1) = 60 pF

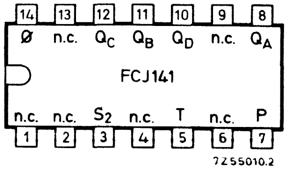
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE ASYNCHRONOUS 10-COUNTER



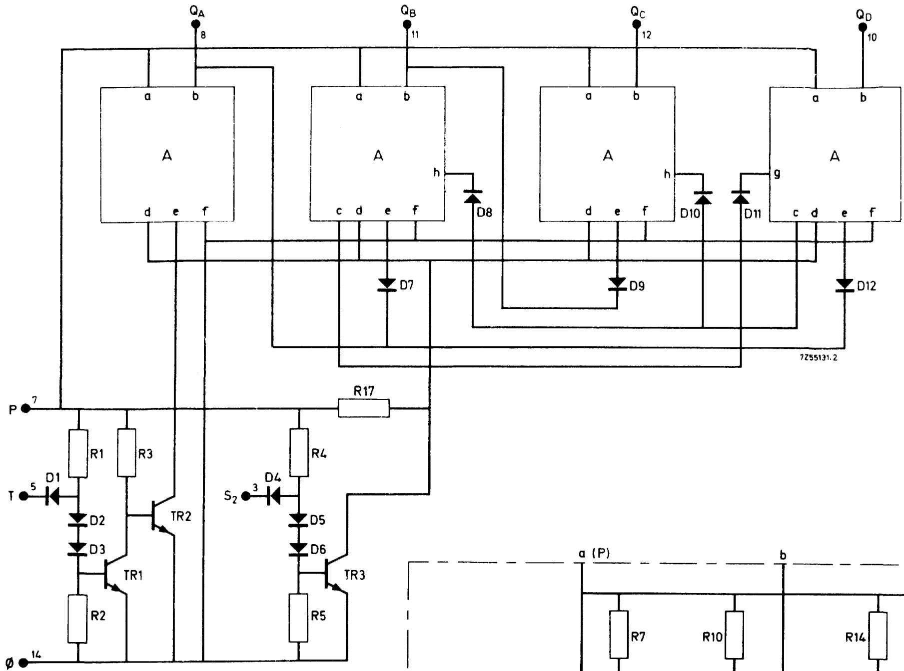


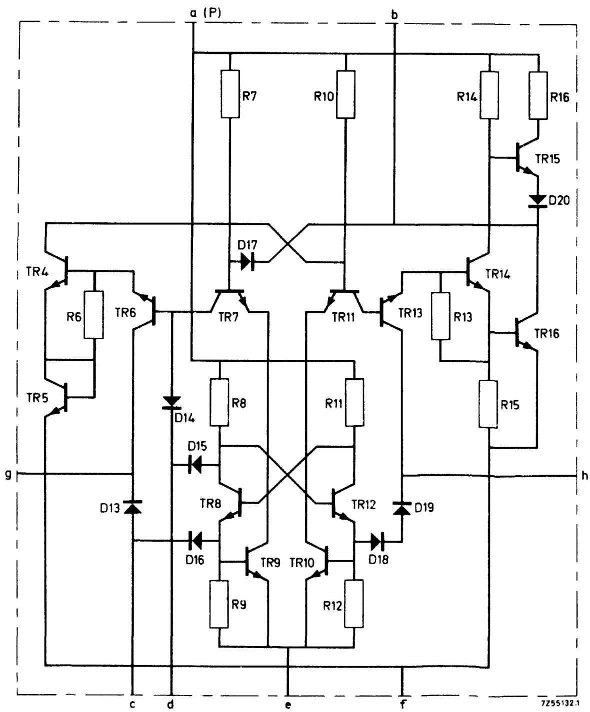
QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan out T_{amb} = 25 °C	N_a	≥ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 180	mW

The FCJ141 is four master-slave flip-flops interconnected to form an a-synchronous decade counter in the 8-4-2-1 code. The information is transferred to the master when the trigger signal is HIGH (the first flip-flop is triggered by the count input at T). When the trigger signal is LOW the information is transferred to the slaves and appears at the outputs. A common reset input S_2 directly resets the outputs and overrides the T input.

PACKAGE OUTLINE: **14 lead plastic dual in-line (type A)** (See General Section)

CIRCUIT DIAGRAMS





block A

FUNCTION TABLES

Count	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

S_2	Q_D	Q_C	Q_B	Q_A
L	count			
H	L	L	L	L

Input S when being at the HIGH state overrides the count input and directly resets all outputs in the LOW state

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Input voltage	$V_T; V_S$	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input current [1]	$-I_S; -I_T$	max.	20	mA
Output current [2]	$-I_Q$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	-35 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

1) At this limit, input voltage typ. -1.5 V.

2) For negative output voltage in LOW state.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	^{o}C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out	N_a	$\geq$	8	
D.C. noise margin				
to T input	M_L	min.	0.4	V
	M_H	min.	1.6	V
to S input	M_L	min.	0.4	V
	M_H	min.	1.6	V
Average propagation delay time T input to Q_3 output	t_{pd}	typ.	200	ns
Clock rate	f_c	max.	3.5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	4	pF
for S input	C_S	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	max.	46	mA
Power dissipation at $T_{amb} = 75\,^{o}C$	P_{tot}	max.	270	mW

CHARACTERISTICS

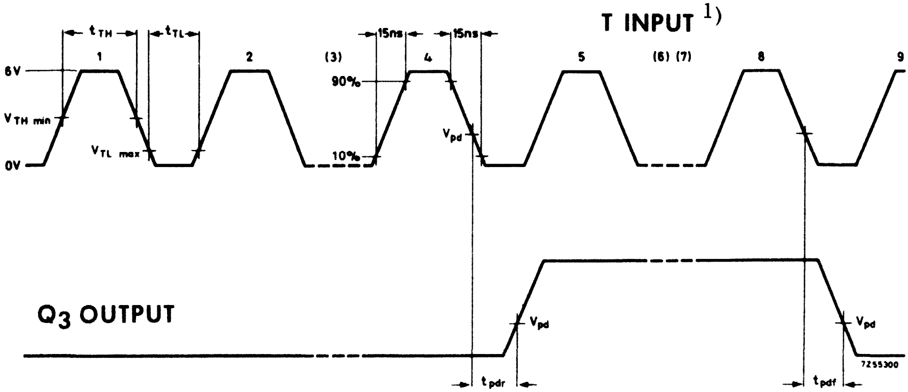
		T_{amb} (°C) 0	25	75		Conditions and references V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QL} max.	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	
	I_{QLmax}	16.0	15.2	14.4	mA	6.3	
Output voltage HIGH	V_{QH} min.	3.8	3.9	4.1	V	5.7	
at: Output current HIGH	$-I_{QH}$	100	100	100	μA	5.7	
Output voltage HIGH (lowest permissible)	V_{QHP} min.	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{TL}$ max.	1.75	1.65	1.55	mA	5.7	$V_T = V_S = 0.4$ V
	$-I_{SL}$ max.	1.75	1.65	1.55	mA	5.7	
	$-I_{TL}$ max.	2.0	1.9	1.8	mA	6.3	
	$-I_{SL}$ max.	2.0	1.9	1.8	mA	6.3	
Input current HIGH	I_{TH} max. I_{SH} max.	1.0	1.0	25.0	μA	5.7	$V_T = V_S = 5.3$ V
Supply current	I_{Pmax}	–	45	40	mA	6.3	$V_T = 0$ V V_S = floating

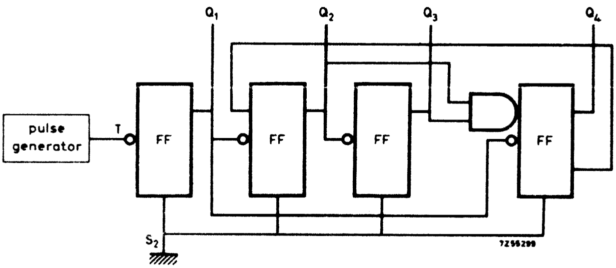
CHARACTERISTICS (continued)

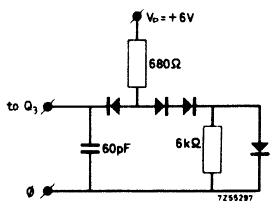
STATIC AND DYNAMIC DATA		T_{amb} (°C) 0	25	75		Conditions and references V_P (V)	
Reset input active HIGH level at S	V_{SHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
to be present during	t_{SHmin}	100	100	140	ns		
Reset input inactive LOW level at S	V_{SLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Change of state of the master of the lowest order flip-flop HIGH level at T	V_{THmin}	2.3	2.2	2.1	V	5.7 and 6.3	
to be present during	t_{THmin}	-	100	-	ns		
Change of state of the slave of the lowest order flip-flop							
Slope of falling edge at T	$(-\frac{dt}{dV})_{Tmax}$	1	1	1	µs/V		
LOW level at T	V_{TLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
to be present during	t_{TLmin}	100	100	140	ns		
Propagation delay times from T to Q3							
Propagation delay reference level	V_{pd}		1.5		V		
Rise propagation delay time	$t_{pdr\ max}$	-	200	-	ns	6.0	
Fall propagation delay time	$t_{pdf\ max}$	-	200	-	ns	6.0	

CHARACTERISTICS (continued)

DYNAMIC DATA



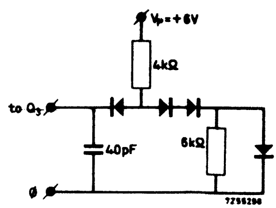




diodes FCY101

C_L 2) = 60 pF

Equivalent load for N = 6



diodes FCY101

C_L 2) = 40 pF

Equivalent load for N = 1

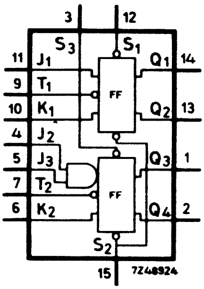
---

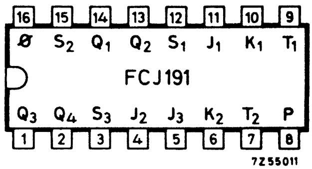
1) The falling edge of the T input signals is max. 1 μs/V

2) Including jig and probe capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP-FLOP



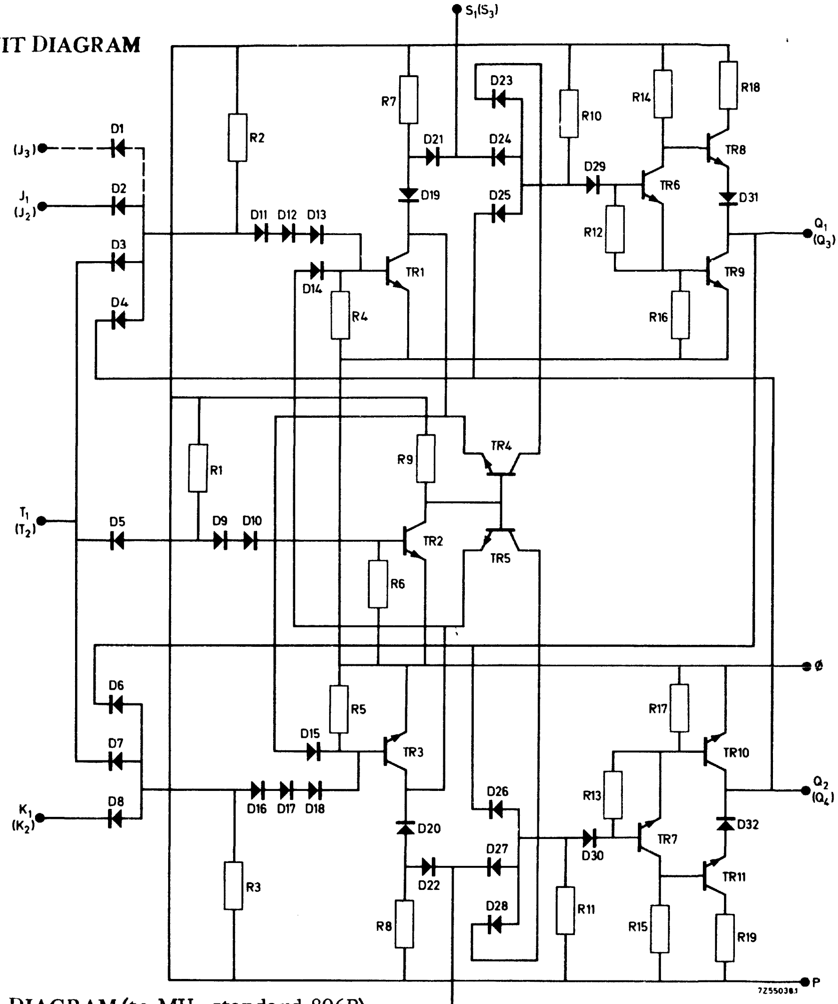


QUICK REFERENCE DATA				
Supply voltage	V_P		6.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Clock rate	f_c	typ.	7	MHz
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	≥	8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ.	1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ.	100	mW

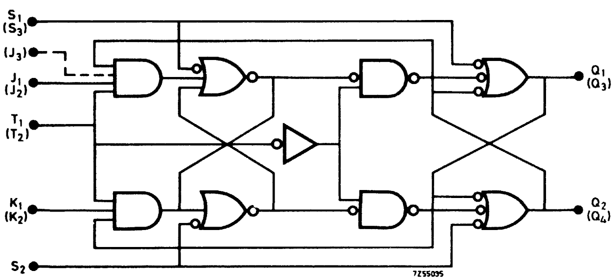
The FCJ191 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, e.g. rise and fall times of all input signals including the trigger signal are immaterial. The set and reset inputs (overriding any other inputs) are active at the LOW level. Typical applications include counters and shift registers.

PACKAGE OUTLINE 16 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 / J	K_1 / K_2	Q_1 / Q_3	Q_2 / Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1, S_2 and S_3 should be HIGH or floating.

For the flip-flop with two J-inputs is $J = J_2 \cdot J_3$ for positive logic

2. Set or reset via S terminals

S_1 / S_3	S_2 / S_2	Q_1 / Q_3	Q_2 / Q_4
H	L	L	H
L	H	H	L
L	L	H	H
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

[1]) For negative output voltage in LOW state.
[2]) At this limit input voltage typ. : −1.5V

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to T input	N_{aT}	⩾	3	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS2}	⩾	2	
	$N_{aS1} = N_{aS3}$	⩾	4	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	12	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_{S2}	typ.	16	pF
	$C_{S1} = C_{S3}$	typ.	8	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1]) Both flip-flops together

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	16.5	12.4	mA	5.7	
		16.0	19.0	14.4	mA	6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	I_Q = −100 μA
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4	1.3	1.2	mA	5.7	$V_J = V_K = 0.4$ V; other inputs floating
		1.6	1.5	1.4	mA	6.3	
	$-I_{TLmax}$	4.0	3.8	3.5	mA	5.7	$V_T = 0.4$ V; other inputs floating
		4.5	4.2	3.9	mA	6.3	
	$-I_{S2Lmax}$	5.7	5.5	5.2	mA	5.7	$V_S = 0.4$ V; other inputs floating
		6.6	6.3	5.8	mA	6.3	
	$-I_{S1Lmax}$, $-I_{S3Lmax}$	2.9	2.8	2.6	mA	5.7	$V_S = 0.4$ V; other inputs floating
		3.3	3.2	2.9	mA	6.3	
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	3	3	75	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{S2Hmax}	4	4	100	μA	5.7	$V_S = 5.3$ V other inputs 0 V
	I_{S1Hmax}, I_{S3Hmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	–	26.7	–	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		V_P (V)	Conditions and references	fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
during: Input time HIGH	t_{THmin}	60	60	60	ns			1
to: T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	-	90	-	ns	6.0	V_{pd} = 1.5 V; N = 1; C_L = 60 pF	4
Fall propagation delay time	$t_{pdf\,max}$	-	120	-	ns	6.0	V_{pd} = 1.5; N = 8; C_L = 60 pF; other output: N = 1; C_L = 60 pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

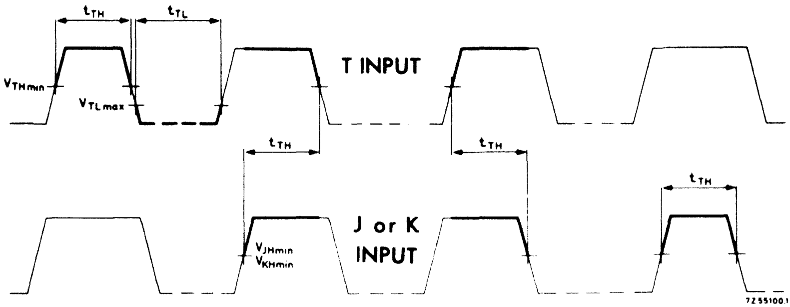


Fig. 1. Waveforms illustrating conditions for change of state.

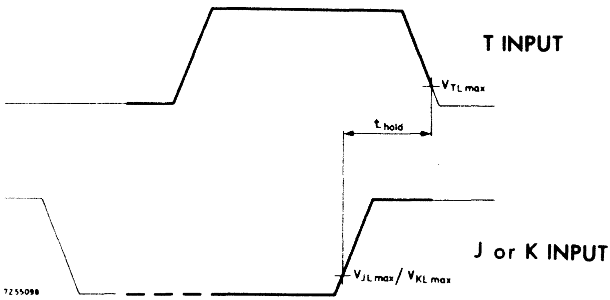


Fig. 2. Waveforms illustrating conditions for no change of state.

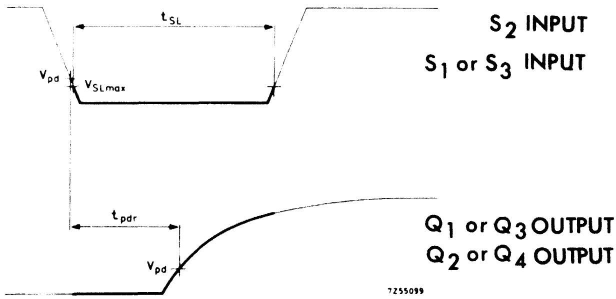
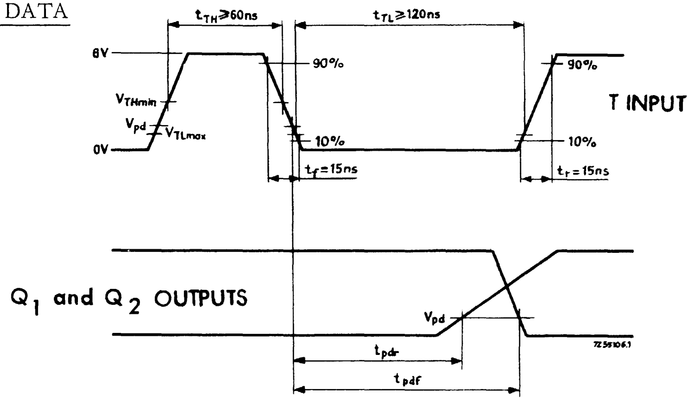
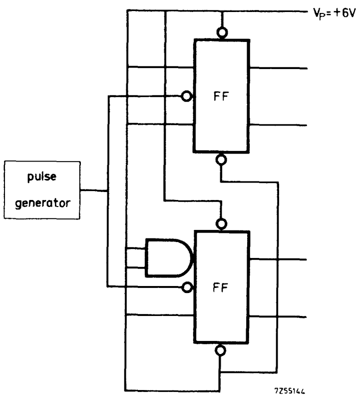


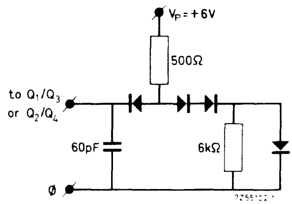
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

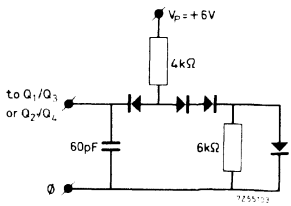
DYNAMIC DATA







Diodes FCY101
Equivalent load for N = 8 and
C_L 1) = 60 pF



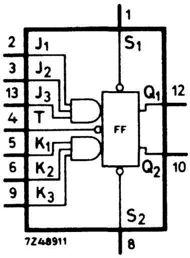
Diodes FCY101
Equivalent load for N = 1 and
C_L 1) = 60 pF

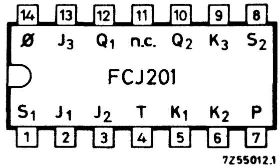
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf} .

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK MASTER-SLAVE FLIP-FLOP



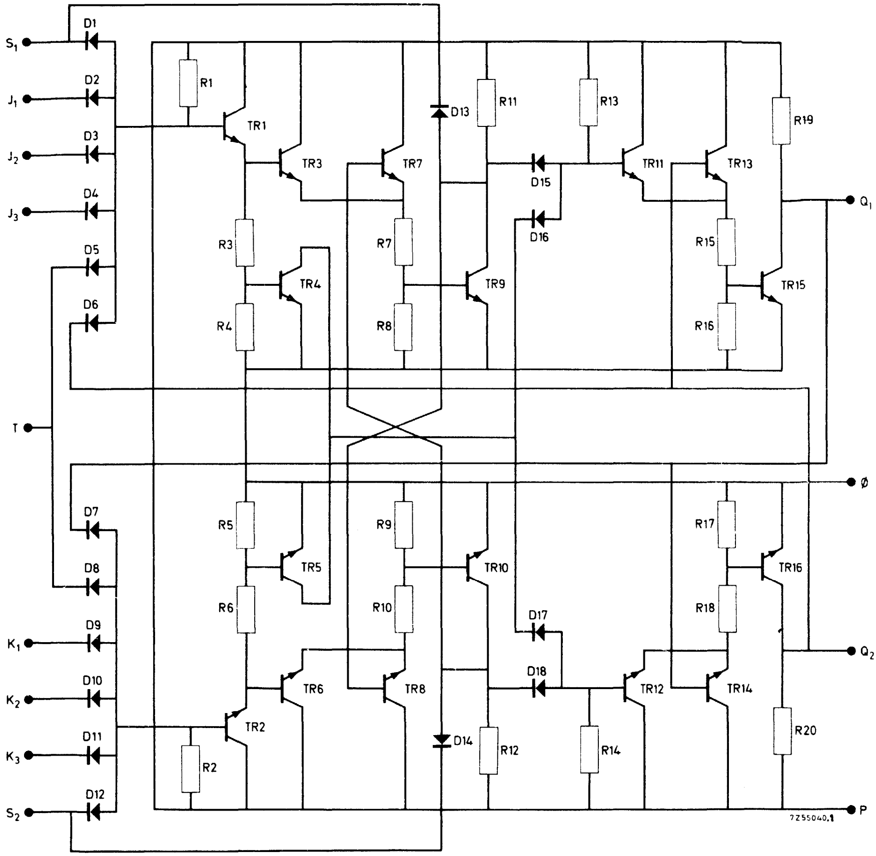


QUICK REFERENCE DATA				
Supply voltage	V_P		6.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Clock rate	f_c	typ.	5	MHz
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	≥	8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ.	1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ.	67	mW

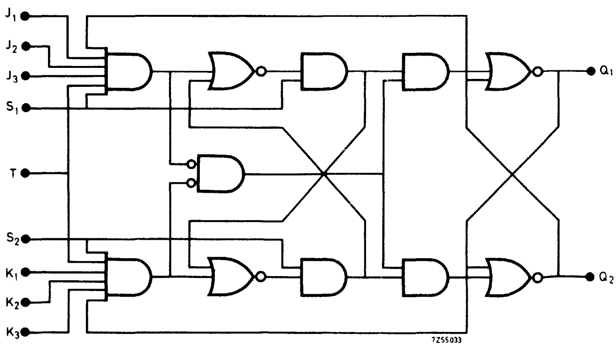
The FCJ201 is a direct-coupled JK flip-flop, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signal, are immaterial. The J, K and T inputs are logically equivalent, allowing the use of J and K for triggering. The direct set inputs (overriding any other inputs) are active at the LOW level.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J	K	Q_1	Q_2
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1 and S_2 should be HIGH or floating.

$J = J_1.J_2.J_3$; $K = K_1.K_2.K_3$ (for positive logic)

2. Trigger action via J and K terminals

J	K	Q_1	Q_2
H→L	X	H	L
X	H→L	L	H
H→L	H→L	reversed	

$J = J_1.J_2.J_3$; $K = K_1.K_2.K_3$
(for positive logic)

If J or K go LOW with T HIGH, Q_1 and Q_2 assume the state shown. If both J and K go LOW with T HIGH, the outputs of Q_1 and Q_2 are reversed (exactly as if J and K remained HIGH and T were triggered).
When triggering on J and K the T input requirements V_{TH} and V_{TL} (see CHARACTERISTICS) apply to J and K.
S_1 and S_2 should be HIGH or floating.

3. Set or reset via S terminals

S_1	S_2	Q_1	Q_2
H	L	L	H
L	H	H	L
L	L	indeterminate	
H	H	no change	

The set inputs override the other inputs and directly determine the output of the flip-flop.
In the case of both set inputs going LOW the first to reach LOW will determine the output conditions.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) [1])

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2])	$-I_Q$	max.	20	mA
Input current [3])	$-I_J$, $-I_K$, $-I_T$, $-I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}		-55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

[1]) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
[2]) For negative output voltage.
[3]) At this limit input voltage type.: -1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to T input	N_{aT}	⩾	4	
to J or K input	$N_{aJ} = N_{aK}$	⩾	8	
to S input	N_{aS}	⩾	5	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.5	V
	M_H	min.	1.9	V
to J or K input	M_L	min.	0.9	V
	M_H	min.	1.9	V
to S input	M_L	min.	0.4	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	2.3	V
Average propagation delay time	t_{pd}	max.	150	ns
Maximum clock rate	f_c	⩾	3	MHz
Equivalent input capacitances				
for T input	C_T	typ.	8	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	8	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	11.2	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	110	mW

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	
		16.0	15.2	14.4	mA	6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.4	5.3	V	5.7	$I_Q = 0$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.9	3.5	2.8	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	350	450	550	μA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.75	1.65	1.55	mA	5.7	$V_J = V_K = 0.4$ V; other inputs floating
		2.0	1.9	1.8	mA	6.3	
	$-I_{TLmax}$	3.5	3.3	3.1	mA	5.7	$V_T = 0.4$ V; other inputs floating
		4.0	3.8	3.6	mA	6.3	
	$-I_{SLmax}$	2.7	2.6	2.4	mA	5.7	$V_S = 0.4$ V; other inputs floating
		3.0	2.9	2.7	mA	6.3	
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	2	2	50	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	20	–	mA	6.3	J, K, S,T inputs HIGH

CHARACTERISTICS

		T_{amb} (°C) 0 +25 +75	V_P (V)	Conditions and references	fig.
DYNAMIC DATA			5.7 and 6.3		
Change of state					
Input voltage HIGH	V_{THmin} V_{JHmin} V_{KHmin}	3.1 2.9 2.5 V		HIGH level at T and J and/or K to be present simultaneously	1
during: T-input time HIGH	t_{THmin}	100 100 100 ns			1
to: Input voltage LOW	V_{TLmax}	1.3 1.1 0.9 V		$t_{TLmin} = t_{pdr}$	1
No change of state					
JK input voltage LOW	V_{JLmax} V_{KLmax}	1.8 1.6 1.3 V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection					
Hold time	$t_{holdmax}$	20 20 20 ns			2
Set or Reset					
S input voltage LOW	V_{SLmax}	1.2 1.0 0.8 V		active $t_{SLmin} = t_{pdr}$	3
S input voltage HIGH	V_{SHmin}	3.1 2.9 2.5 V		inactive	
DYNAMIC DATA					
Propagation delay times from T to Q					
Rise propagation delay time	t_{pdrmax}	- 200 - ns		V_{pd} = 1.5 V N = 1; C_L = 60 pF other output N = 8; C_L = 56 pF	4
Fall propagation delay time	t_{pdfmax}	- 100 - ns		V_{pd} = 1.5 V N = 8; C_L = 56 pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

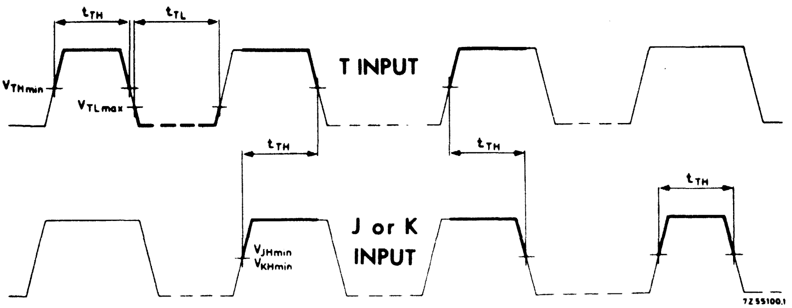


Fig. 1. Waveforms illustrating conditions for change of state.

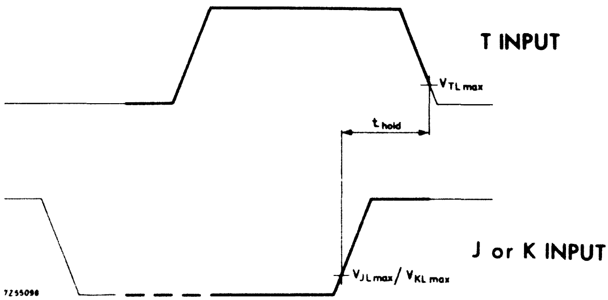


Fig. 2. Waveforms illustrating conditions for no change of state.

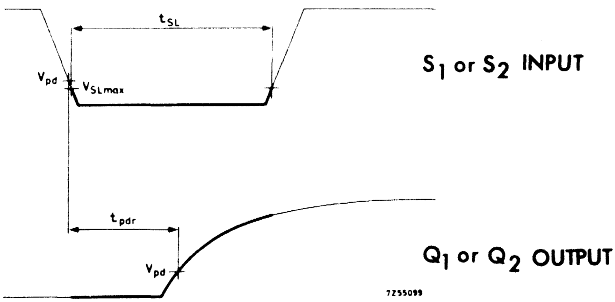
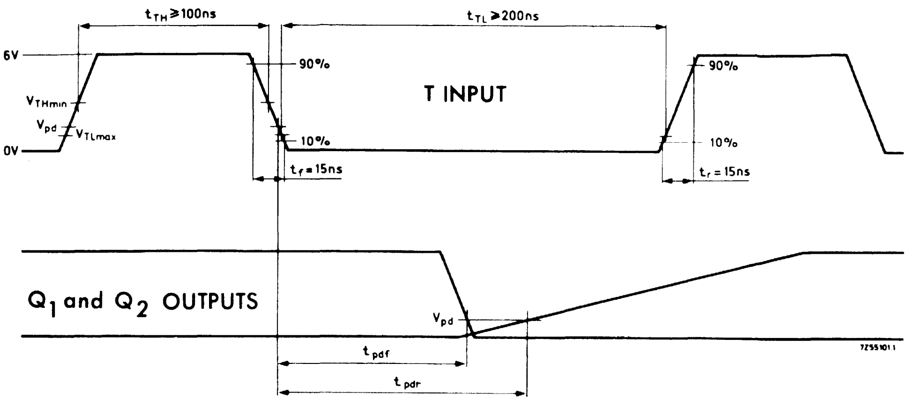
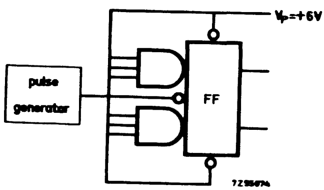


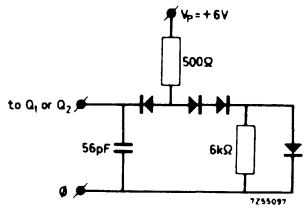
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

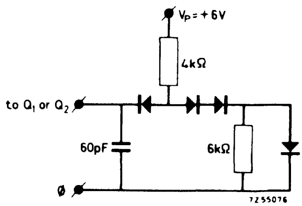






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 56 pF



diodes FCY101

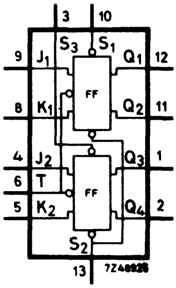
Equivalent load for N = 1 and C_L[1]) = 60 pF

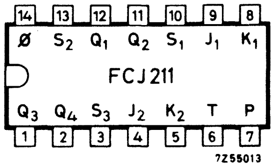
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf} .

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER SLAVE FLIP-FLOP



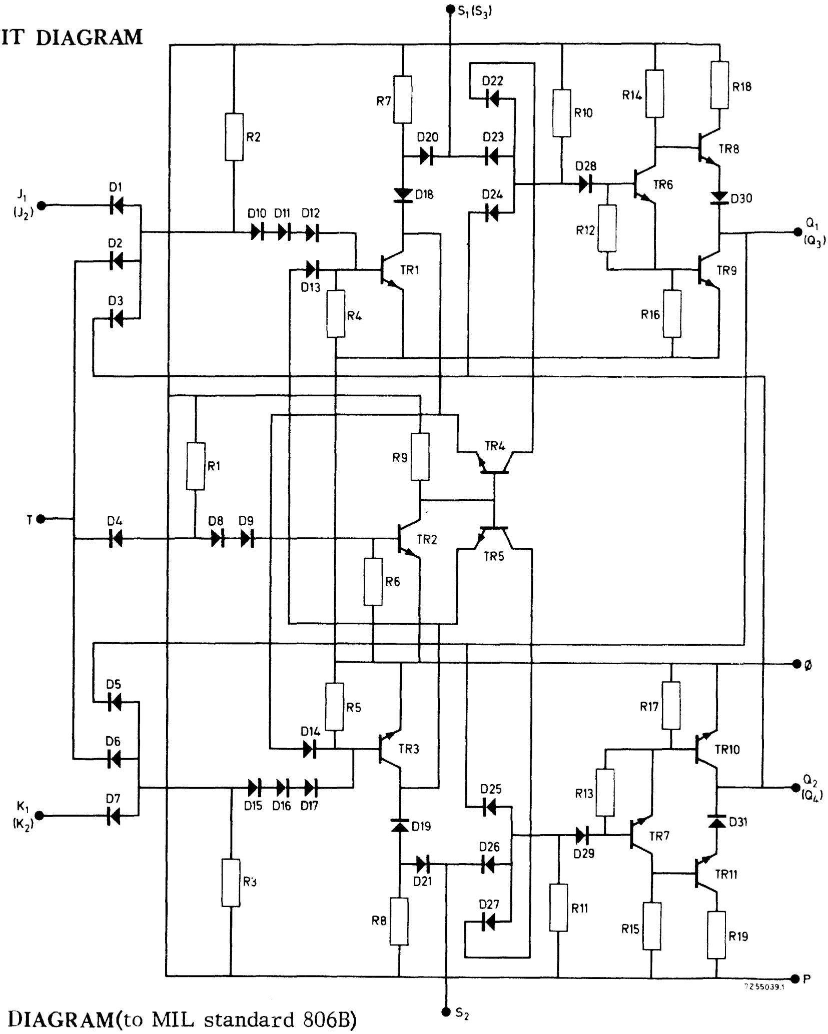


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	≥ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 100	mW

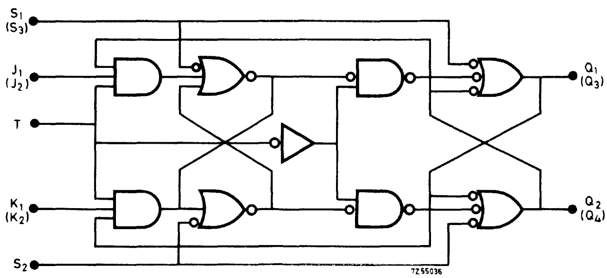
The FCJ211 comprises two independent direct-coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including trigger signals, are immaterial. The set and reset inputs (overriding any other inputs) are active at the LOW level. Typical applications include synchronous counters and shift registers.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM(to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 / J	K_1 / K_2	Q_1 / Q_3	Q_2 / Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1, S_2 and S_3 should be HIGH or floating.

2. Set or reset via S terminals

S_1 / S_3	S_2 / S_4	Q_1 / Q_3	Q_2 / Q_4
H	L	L	H
L	H	H	L
L	L	H	H
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

[1]) For negative output voltage in LOW state.
[2]) At this limit input voltage typ. −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	^oC
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to T input	N_{aT}	≥	1	
to J or K input	$N_{aJ} = N_{aK}$	≥	10	
to S input	N_{aS2}		2	
	$N_{aS1} = N_{aS3}$		4	
to G input	N_{aG}	≥	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	≥	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	24	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_{S2}	typ.	16	pF
	$C_{S1} = C_{S3}$	typ.	8	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at $T_{amb} = 75\ ^oC$ [1]	P_{tot}	max.	150	mW

[1]) Both flip-flops together

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	16.5 19.0	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	I_Q = −100 μA
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4 1.6	1.3 1.5	1.2 1.4	mA mA	5.7 6.3	$V_J = V_K$ = 0.4 V; other inputs floating
	$-I_{TLmax}$	8.0 9.0	7.6 8.4	7.0 7.8	mA mA	5.7 6.3	V_T = 0.4 V; other inputs floating
	$-I_{S2Lmax}$	5.7 6.6	5.5 6.3	5.2 5.8	mA mA	5.7 6.3	V_S = 0.4 V; other inputs floating
	$-I_{S1Lmax}$, $-I_{S3Lmax}$	2.9 3.3	2.8 3.2	2.6 2.9	mA mA	5.7 6.3	V_S = 0.4 V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K$ = 5.3 V other inputs 0 V
	I_{THmax}	6	6	150	μA	5.7	V_T = 5.3 V other inputs 0 V
	I_{S2Hmax}	4	4	100	μA	5.7	V_S = 5.3 V other inputs 0 V
	$-I_{S1Hmax}$ $-I_{S3Hmax}$	2	2	50	μA	5.7	V_S = 5.3 V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	-	26.7	-	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
during: Input time HIGH	t_{THmin}	60	60	60	ns			1
to: T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	-	90	-	ns	6.0	V_{pd} = 1.5 V; N = 1; C_L = 60 pF	4
Fall propagation delay time	$t_{pdf\,max}$	-	120	-	ns	6.0	V_{pd} = 1.5; N = 8; C_L = 60 pF; other output: N = 1; C_L = 60 pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

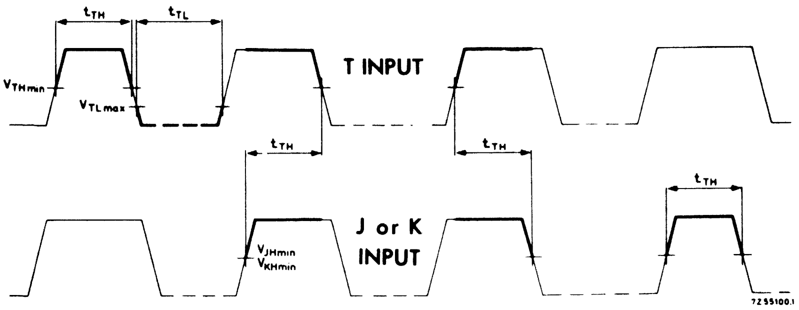


Fig. 1. Waveforms illustrating conditions for change of state.

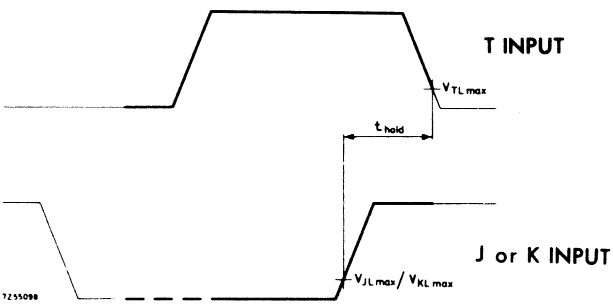


Fig. 2. Waveforms illustrating conditions for no change of state.

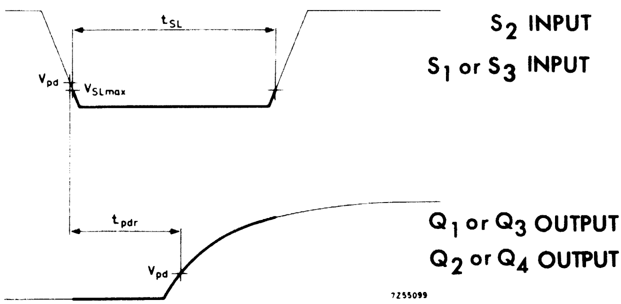
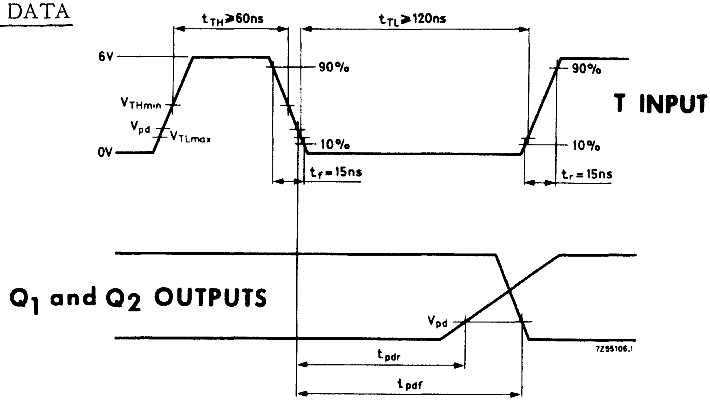
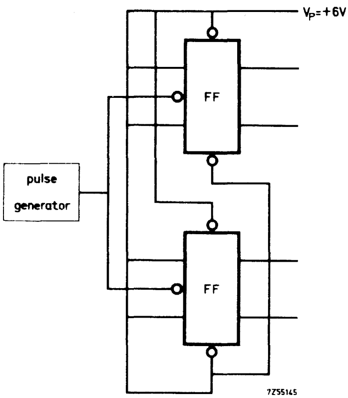


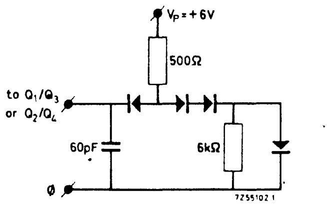
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

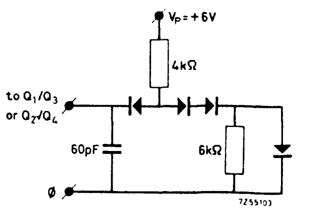
DYNAMIC DATA







Diodes FCY101
Equivalent load for N = 8 and
C_L[1]) = 60 pF

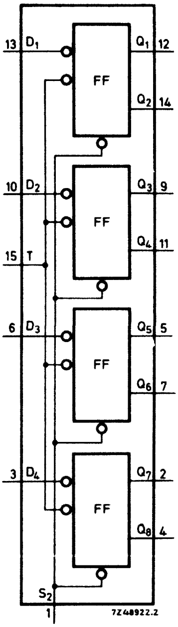


Diodes FCY101
Equivalent load for N = 1 and
C_L[1]) = 60 pF

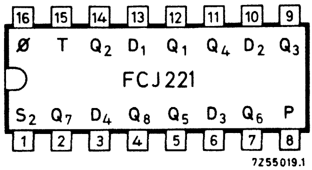
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.



QUADRUPLE LATCH FLIP-FLOP

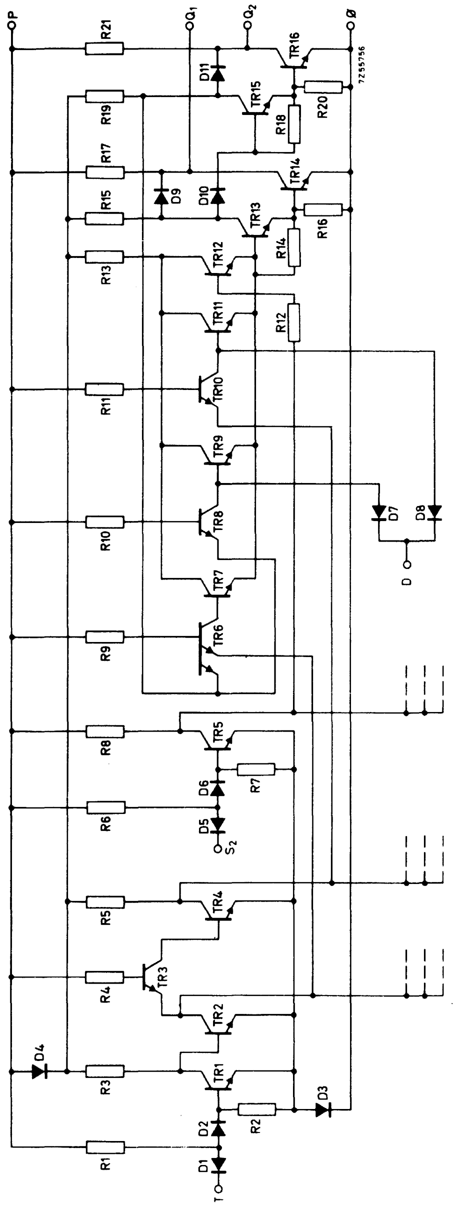


PACKAGE OUTLINE
16 lead plastic dual in-line (type A)
See General Section

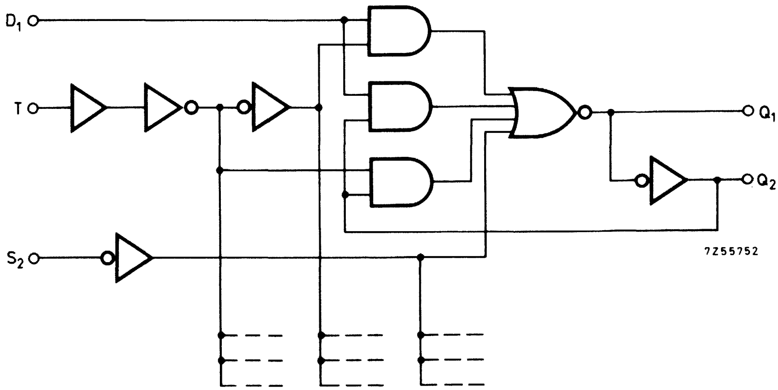
QUICK REFERENCE DATA				
Supply voltage	V_P	6.0	± 5%	V
Operating ambient temperature range	T_{amb}	0 to	+75	°C
Clock rate at T_{amb} = 25 °C	f_c	typ.	5	MHz
Available d.c. fan out T_{amb} = 25 °C	N_a	≥	10	
D.C. noise margin T_{amb} = 25 °C	M_L	typ.	1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ.	250	mW

The FCJ221 is a quadruple latch flip-flop with D inputs, a common clock (T) and a reset input (S_2).
A LOW input signal at D arrives after the last T signal goes HIGH at output Q_1.
The information follows after a LOW signal at the T input.
It is possible to influence the output state of the flip-flop.

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTION

Function tables

t_n	t_{n+1}
D	Q1
H	L
L	H

S2	Q1
L	L
H	X

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
t_n = bit time before trigger pulse
t_{n+1} = bit time after trigger pulse
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage at $T_{amb} < 40\ ^{o}C$	V_P	max.	8	V
Output voltage	V_Q	max.	8	V
Input voltage	V_G	max.	8	V
Input current	$-I_D$; $-I_T$; $-I_{S2}$	max.	20	mA [1]
Storage temperature	T_{stg}	−55 to	+125	^{o}C
Operating ambient temperature	T_{amb}	0	+75	^{o}C

[1]) At negative input voltage

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	^oC
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan-out	N_a	≥	10	
D.C. noise margin to D input	M_{DL}	min.	0.2	V
	M_{DH}	min.	3.0	V
to T, S_2 input	M_{TL}; M_{S2L}	min.	0.3	V
	M_{TH}; M_{S2H}	min.	3.1	V
Supply current	I_{Pav}	max.	47	mA[1])
Power dissipation at T_{amb} = 75 ^oC	P_{tot}	max.	300	mW

[1]) Input open and V_D = 0 V

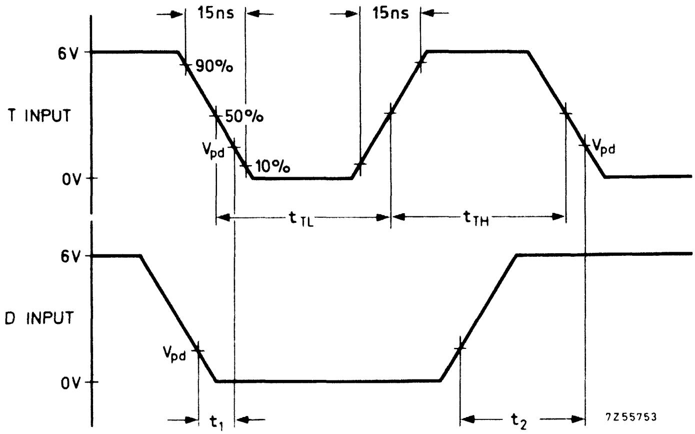
CHARACTERISTICS

STATIC DATA		Tamb (°C) 0	25	75		V_P (V)	Conditions and references
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at:							
Output current LOW	I_{QLmax}	17.5	16.5	15.5	mA	5.7	
		20.0	19.0	18.0	mA	6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7	$-I_Q = 0$
Input voltage LOW							
D	V_{DLmax}	0.9	0.8	0.6	V	5.7 and 6.3	
T; S_2	V_{TLmax} V_{S2Lmax}	1.0	0.9	0.7	V	5.7 and 6.3	
Input voltage HIGH							
D	V_{DHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
T; S_2	V_{THmin} V_{S2Hmin}	2.2	2.1	2.0	V	5.7 and 6.3	
Input current LOW							
D	$-I_{DLmax}$	2.55	2.5	2.45	mA	5.7	$V_D = 0.4$ V
T; S_2	$-I_{TLmax}$ $-I_{S2Lmax}$	1.75	1.65	1.55	mA	5.7	$V_T = V_{S2} = 0.4$ V
D	$-I_{DLmax}$	2.85	2.8	2.75	mA	6.3	$V_D = 0.4$ V
T; S_2	$-I_{TLmax}$ $-I_{S2Lmax}$	2.0	1.9	1.8	mA	6.3	$V_T = V_{S2} = 0.4$ V
Input current HIGH							
D	I_{DHmax}	2	2	50	µA	6.3	$V_D = V_P$
T; S_2	I_{THmax} I_{S2Hmax}	1	1	25	µA	6.3	$V_T = V_{S2} = V_P$
Output current changing output state							
Q_1	$-I_{Q1max}$	4.2	4.05	3.75	mA	6.3	$V_Q = 0.4$ V
Q_2	$-I_{Q2max}$	6.3	6.1	5.65	mA	6.3	$V_Q = 0.4$ V
Supply current	I_{Pmax}	–	–	47	mA	6.3	$V_D = 0$ V; T and S_2 inputs open

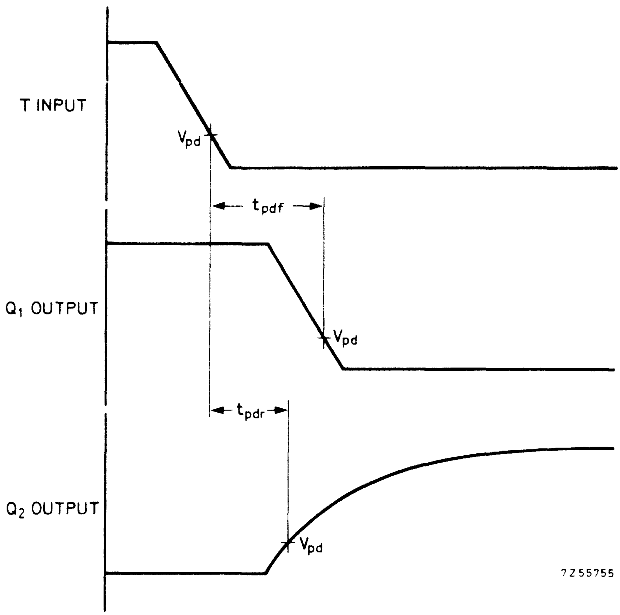
CHARACTERISTICS

		Tamb (°C)				Conditions and references	
		0	25	75		Vp (V)	
STATIC DATA							
D.C. noise margin							
LOW: D	M_{DLmin}	0.5	0.4	0.2	V		
T; S_2	M_{TLmin} / M_{S2Lmin}	0.6	0.5	0.3	V		
HIGH: D	M_{DHmin}	3.0	3.1	3.2	V		
T; S_2	M_{THmin} / M_{S2Hmin}	3.1	3.2	3.3	V		
DYNAMIC DATA							
Input time LOW T	t_{TLmin}	-	100	-	ns	5.7 and 6.3	
Input time HIGH T	t_{THmin}	-	70	-	ns	5.7 and 6.3	
Input time LOW S_2	t_{S2Lmin}	-	100	-	ns	5.7 and 6.3	
S_2 (changing output state)	t_{S2Lmin}	-	100	-	ns	5.7 and 6.3	
Set-up times:						5.7 and 6.3	
t_1	t_{su1min}	-	0	-	ns		
t_2	t_{su2min}	-	30	-	ns		
Propagation delay times:							
Rise propagation delay times							
T → Q_1	t_{pdrmax}	-	95	-	ns	6.0	N = 1; C_L = 40 pF; V_{pd} = 1.5 V
T → Q_2	t_{pdrmax}	-	105	-	ns	6.0	
S_2 → Q_2	t_{pdrmax}	-	85	-	ns	6.0	
Fall propagation delay times							
T → Q_1	t_{pdfmax}	-	60	-	ns	6.0	N = 8; C_L = 70 pF; V_{pd} = 1.5 V
T → Q_2	t_{pdfmax}	-	120	-	ns	6.0	
S_2 → Q_2	t_{pdfmax}	-	60	-	ns	6.0	

CHARACTERISTICS (continued)

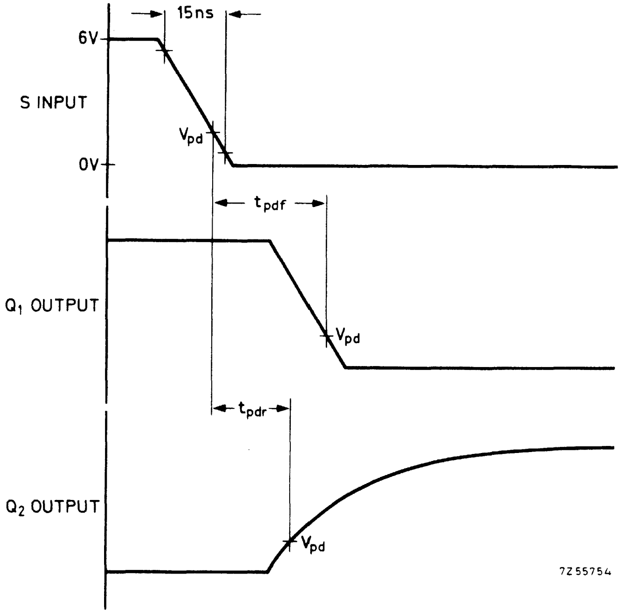


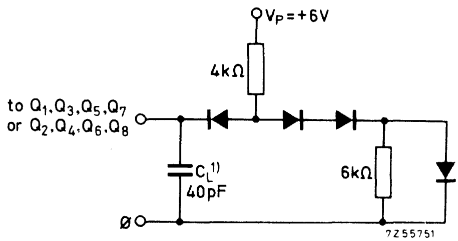
Waveform illustrating conditions for change of state



Waveforms illustrating t_{pdr} and t_{pdf}

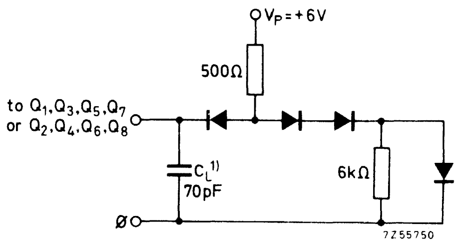
CHARACTERISTICS (continued)





diodes FCY101

N = 1



diodes FCY101

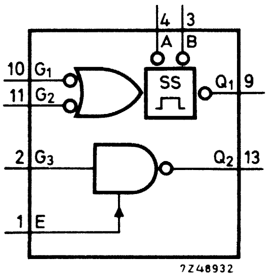
N = 8

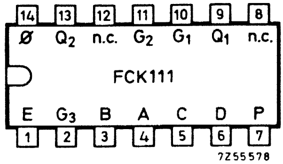
Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

1) Including jig and probe capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

MONOSTABLE MULTIVIBRATOR





QUICK REFERENCE DATA

Supply voltage	V_P		6.0 ± 5%	V
Operating ambient temperature	T_{amb}		0 to +75	°C
Propagation delay time $G_1 \rightarrow Q_1$	t_{pdf}	typ.	70	ns
$T_{amb} = 25\ ^oC$ at $V_{pd} = 1.5\ V$ $G_3 \rightarrow Q_2$	t_{pdf}	typ.	40	ns
Output pulse width: $R_t = 10\ k\Omega \pm 1\%$; $C_t = 160pF \pm 1\%$	t_{Q1L}	typ.	1.0	μs
Available d.c. fan-out Q_1	N_a	≥	14	
$T_{amb} = 0$ to $+75\ ^oC$ Q_2	N_a	≥	14	
A	N_a	=	1	
D.C. noise margin $T_{amb} = 25\ ^oC$	M_L	typ.	1.2	V
Power consumption 50% duty cycle, $T_{amb} = 25\ ^oC$	P_{av}	typ.	58	mW

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

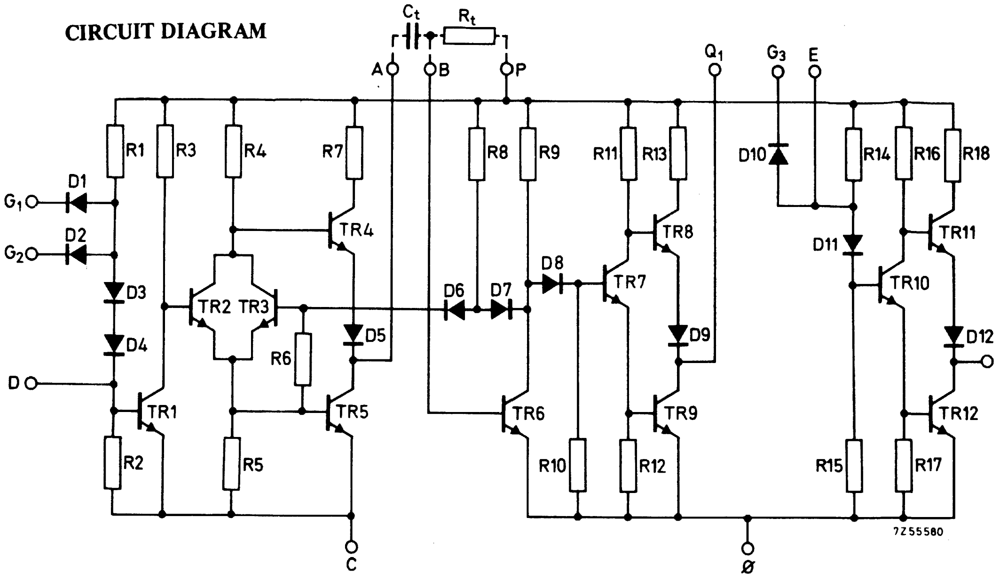
The FCK111 comprises a threshold triggered monostable circuit and an independent expandable inverter.

The monostable function is obtained by an externally connected resistor and capacitor. Each time one of the inputs G_1 or G_2 is going LOW a negative going pulse appears at output Q_1.

The pulse width is adjustable over a very wide range by varying the resistor and capacitor values.

If the input (G_3) of the inverter is connected to A a positive going pulse is obtained at the output Q_2, almost coinciding and practically having the same width as the output pulse Q1, provided that the width of the input pulse does not exceed the width of the output pulse. The outputs Q_1 and Q_2 are bi-directional and have a high fan-out drive capability.

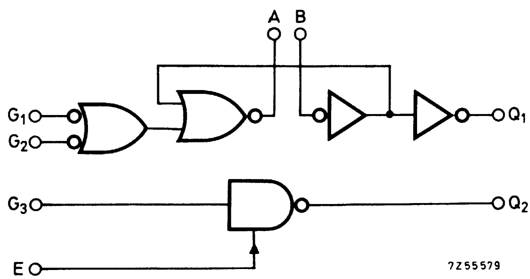
CIRCUIT DIAGRAM



Notes

1. Terminals C and D make the circuit compatible with the FCK101.
2. To ensure conformity with the characteristics given in the data sheets, terminal C must be connected to terminal ϕ.
   If terminals C and ϕ are not interconnected, the output pulse can be shortened by connecting a diode or a voltage source to C (positive to ϕ); however, this will alter a number of characteristics, including special input levels and output level A.
3. The noise margin for a.c. disturbances at the trigger inputs G_1 and G_2 can be increased by connecting a capacitor between terminals C and D, but this reduces the minimum operating frequency.

LOGIC DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current	$-I_Q$	max.	20.0	mA [1]
Input current	$-I_G$	max.	20.0	mA [2]
Voltage difference between any two inputs		max.	8.0	V
Expander input voltages:				
– with respect to supply	$V_P - V_E$	max.	8.0	V
– with respect to other inputs	$V_G - V_E$	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}		-55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C
Output short circuit duration (duty cycle 10%, either output, or both)	t_{Qsc}	max.	60	ms
Timing resistor (R_t connected to 6.3 V)	R_t	min.	5	kΩ
		max.	20	kΩ
Timing capacitor	C_t	max.	160	μF
		min.	30	pF [3]

[1] for negative output voltage in LOW state.

[2] at this limit, input voltage typ: − 1.5 V.

[3] C_t min 30 pF is not a rating, but is to be considered as the minimum value at which the circuit still performs its function.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	^{o}C
Uniform system supply voltage	V_P		5.7 to 6.5	V
Available d.c. fan-out Q_1	N_a	$\geq$	14	
Available d.c. fan-out Q_2	N_a	$\geq$	14	
Available d.c. fan-out A	N_a	=	1	
D.C. noise margin FCK111 → gate	M_L	min.	0.4	V
	M_H	min.	1.2	V
gate → FCK111	M_L	min.	0.4	V
	M_H	min.	1.8	V
Propagation delay time: $G_1 \rightarrow Q_1$	t_{pdf}	max.	170	ns
$G_1 \rightarrow Q_2$	t_{pdr}	max.	200	ns
$G_3 \rightarrow Q_2$	t_{pdr}	max.	120	ns
$G_3 \rightarrow Q_2$	t_{pdf}	max.	55	ns
Equivalent input capacitance	C_G	typ.	4	pF
Supply current (duty cycle 50 %)	I_{Pav}	typ.	10.9	mA
Power dissipation at T_{amb} = 75 ^{o}C	P_{tot}	max.	98	mW
Relative change of output pulse width vs supply voltage	see page 10			
Output pulse width vs timing capacitor (C_t)	see page 10			

CHARACTERISTICS : (pin C connected to pin ϕ)

STATIC DATA		T_{amb} (°C) 0	25	75	Conditions and References V_P (V)	
Output Q_1						
Output voltage LOW at:	$V_{Q1L\,max}$	0.4	0.4	0.4 V	5.7 and 6.3	V_B (pin 3) at 0 V
Output current LOW	$I_{Q1L\,max}$	25 28	27 27	26 mA 26 mA	5.7 6.3	
Output voltage HIGH	$V_{Q1H\,min}$	3.5 2.6	3.7 2.8	4.0 V 2.9 V	5.7 5.7	$-I_{Q1H}$ = 30 μA and $-I_{Q1H}$ = 5 mA; B (pin 3) connected to V_P via 20 kΩ (± 1 %)
Output short circuit current	$-I_{Q1sc\,min}$	16.5	19.5	18.0 mA	5.7	B (pin 3) connected to Vp via 20 kΩ (± 1 %) (max. duration 60 ms; duty cycle 10 %)
Output Q_2						
Output voltage LOW at:	$V_{Q2L\,max}$	0.4	0.4	0.4 V	5.7 and 6.3	
Output current LOW	$I_{Q2L\,max}$	25 28	27 27	26 mA 26 mA	5.7 6.3	
and Input voltage HIGH G_3	$V_{GH\,min}$	2.3	2.2	2.1 V	5.7 and 6.3	
Output voltage HIGH at:	$V_{Q2H\,min}$	3.5 2.6	3.7 2.8	4.0 V 2.9 V	5.7 5.7	$-I_{Q2H}$ = 30 μA $-I_{Q2H}$ = 5 mA
Input voltage LOW G_3	$V_{GL\,max}$	1.0	1.0	0.8 V	5.7 and 6.3	
Output short circuit current	$-I_{Q2sc\,min}$	16.5	19.5	18.0 mA	5.7	$V_{GL\,max}$ (max. duration 60 ms; duty cycle 10 %)

CHARACTERISTICS (continued)

STATIC DATA (continued)		T_{amb} (°C) 0	25	75	V_P (V)	Conditions and references
Output A						
Output voltage LOW	$V_{AL\,max}$	0.4	0.4	0.4 V	5.7 and 6.3	
at: Output current LOW	$I_{AL\,max}$	2.0	2.0	2.0 mA	5.7 and 6.3	see note
and Input voltage LOW; G_1, G_2 or V_B (pin 3) at 0 V	$V_{GL\,max}$	1.0	1.0	0.8 V	5.7 and 6.3	
Output voltage HIGH	$V_{AH\,min}$	3.9	4.0	4.1 V	5.7	$-I_{AH}$ = 30 μA
		3.2	3.4	3.4 V	5.7	$-I_{AH}$ = 5 mA
at: Input voltage HIGH	$V_{GH\,min}$	2.3	2.2	2.1 V	5.7 and 6.3	
or: B (pin 3) connected to V_P via 20 kΩ (± 1 %)						
Output short circuit current	$-I_{Asc\,min}$	30	30	25 mA	5.7	B (pin 3) connected to V_P via 20 kΩ (± 1%) (max. duration 60 ms; duty cycle 10 %)

Note

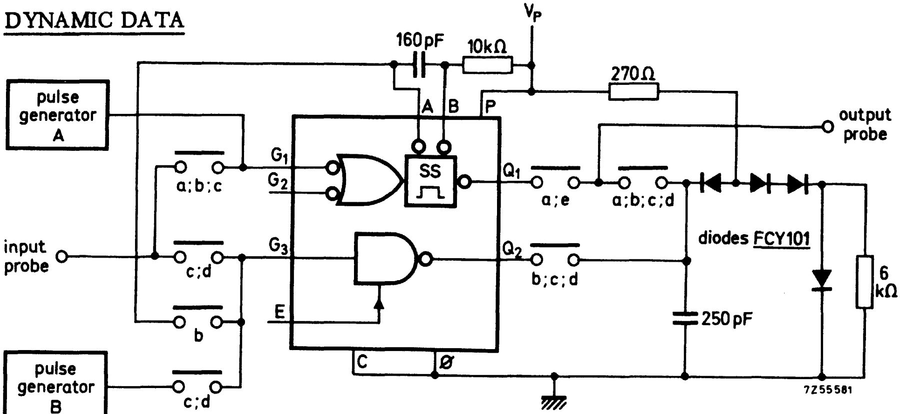
$I_{AL\,max}$ is an extra static current, which can be applied to output A under both static and dynamic conditions without dusturbing the output pulse width.

CHARACTERISTICS (continued)

STATIC DATA (continued)		T_{amb} (°C) 0	25	75		Conditions and references V_P (V)	
Input current LOW	$-I_{GL}$ max	1.75	1.65	1.85	mA	5.7	V_G = 0.4 V other inputs floating
		2.00	1.90	1.80	mA	6.3	V_G = 0.4 V
Input current HIGH	I_{GH} max	1.0	1.0	25.0	μA	5.7	V_G = 5.3 V, other inputs at V_G = 0 V
Supply current (unloaded)							current flow in R_t not included
output Q_1 HIGH, output Q_2 LOW	I_{PH} typ	8.3	8.0	7.5	mA	6.0	
output Q_1 LOW, output Q_2 LOW	I_{PL} typ	13.5	11.3	10.3	mA	6.0	
	I_{PL} max	17.3	16.6	15.6	mA	6.3	
Average supply current	I_{Pav}	14.7	14.1	13.2	mA	6.3	duty cycle 50 %
DYNAMIC DATA							
Propagation delay times							
Rise : $G_1 \rightarrow Q_2$	t_{pdr} max	170	150	200	ns	6.0	V_{pd} = 1.5 V, N = 15, C_L = 250 pF, $t_f = t_r$ = 15 ns
$G_3 \rightarrow Q_2$	t_{pdr} max	80	85	120	ns	6.0	
Fall : $G_1 \rightarrow Q_1$	t_{pdf} max	170	130	170	ns	6.0	
$G_3 \rightarrow Q_2$	t_{pdf} max	55	50	55	ns	6.0	
Pulse width	t_{Q1L}max		1.10		μs	6.0	R_t = 10 kΩ ± 1 %, C_t = 160 pF ± 1 %
	t_{Q1L}typ		1.00		μs	6.0	
	t_{Q1L}min		0.90		μs	6.0	
Duration input LOW	t_{GL} min	30	30	40	ns	5.7 and 6.3	

CHARACTERISTICS (continued)

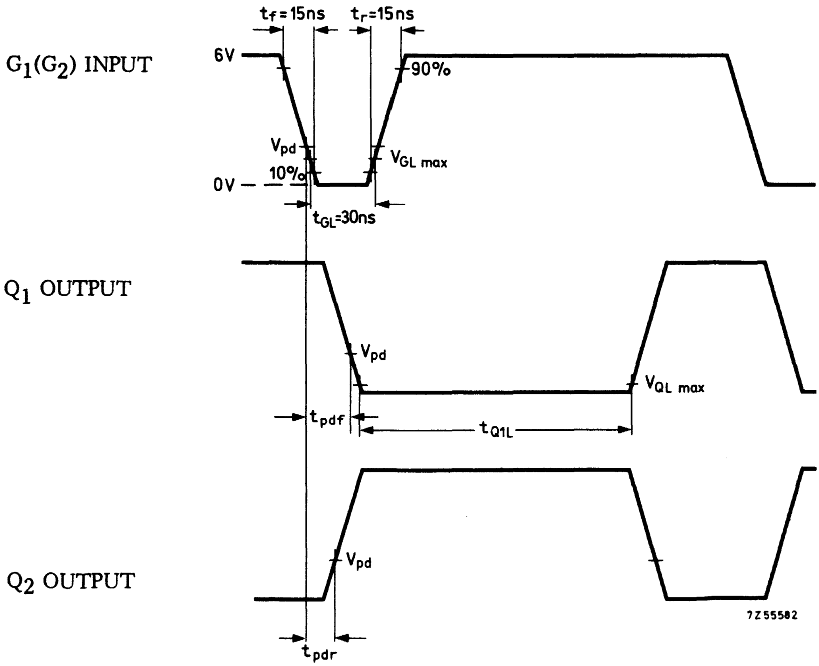
DYNAMIC DATA



Measurement set-up

$a = t_{pdf} : G_1 \rightarrow Q_1$ $\qquad$ $c = t_{pdf} : G_3 \rightarrow Q_2$ $\qquad$ $e = t_{Q1L}$

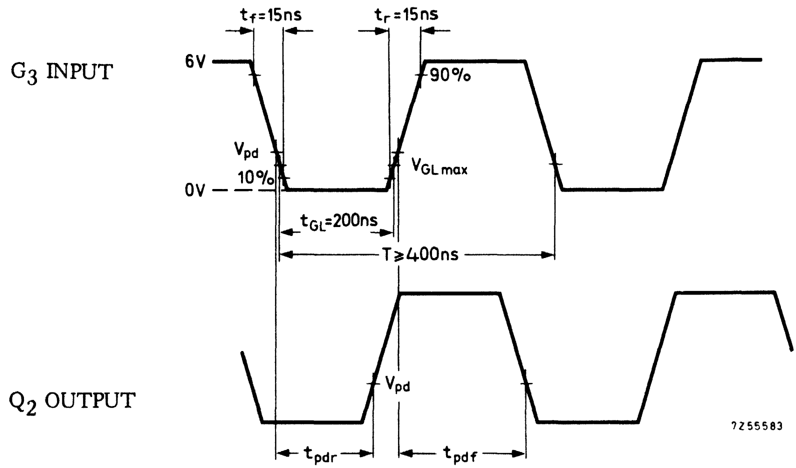
$b = t_{pdr} ; G_1 \rightarrow Q_2$ $\qquad$ $d = t_{pdr} ; G_3 \rightarrow Q_2$



Waveform illustrating measurement of t_{pdr}, t_{pdf}, t_{GL} and t_{Q1L} for A pulse generator.

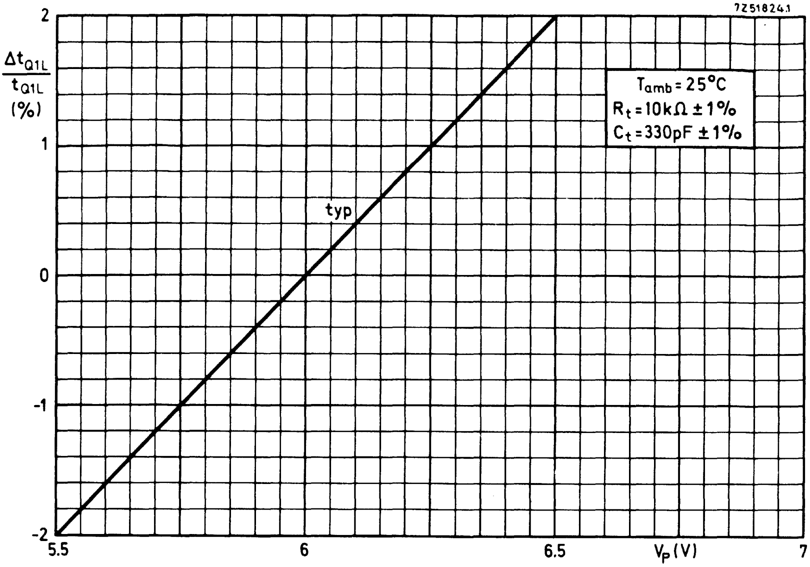
CHARACTERISTICS (continued)

DYNAMIC DATA

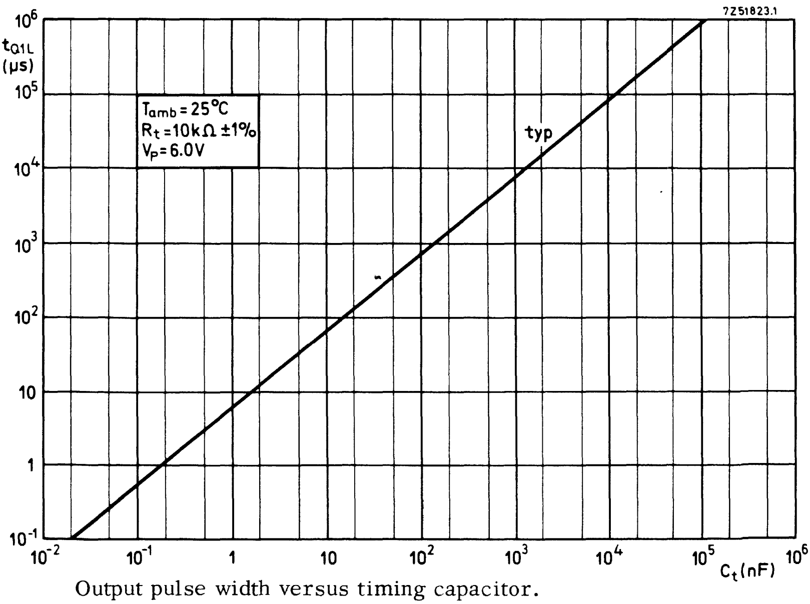


Waveforms illustrating measurement of t_{pdr}, t_{pdf} and t_{GL} for B pulse generator.

CHARACTERISTICS (continued)



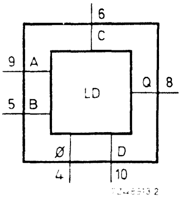
Relative change of output pulse width versus supply voltage.

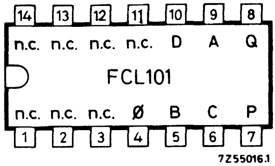


Output pulse width versus timing capacitor.

The FC family of DTL silicon monolithic integrated circuit has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

LEVEL DETECTOR



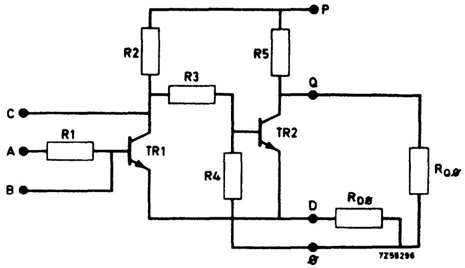


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Input hysteresis voltage $R_{DØ}$ = 100 Ω, T_{amb} = 25 °C	ΔV_{At}	min. 60 max. 200	mV mV
Available output current $R_{DØ}$ = 100 Ω, T_{amb} = 25 °C	I_{QL}	2.7	mA
Operating frequency T_{amb} = 25 °C	f	typ. 5	MHz
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 12	mW

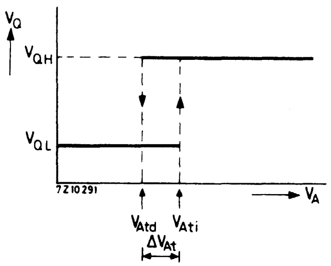
The FCL101 is a non-inverting Schmitt-trigger circuit. Tripping levels are set by an external resistor or zener diode.
Typical applications are discrimination, restoration, level shifting and pulse-shaping (squaring).

PACKAGE OUTLINE 14 lead dual in-line (See General Section)

CIRCUIT DIAGRAM



VOLTAGE TRANSFER CURVE



Letter symbols:

$R_{Q\emptyset}$ = external resistor between Q and Ø

$R_{D\emptyset}$ = external resistor between D and Ø

V_Q = short for $V_{Q\emptyset}$ = voltage at Q with respect to Ø, the common reference and supply return terminal

V_{Ati} = tripping level for increasing input voltage V_A (short for $V_{A\emptyset}$)

V_{Atd} = tripping level for decreasing input voltage V_A

$\Delta V_{At} = V_{Ati} - V_{Atd}$ = input hysteresis voltage.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_A	max.	8.0	V
with respect to supply voltage	$V_A - V_P$	max.	2.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_A$	max.	0.5	mA
Other terminals	I_B	max.	5	mA
	V_C	max.	5.0	V
	V_D	max.	5.0	V
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Output resistance	P_O	max.	7.6	kΩ
Supply current at T_{amb} = 25 °C, V_P = 6 V duty cycle 50%	I_{Pav}	typ.	2.0	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	27	mW

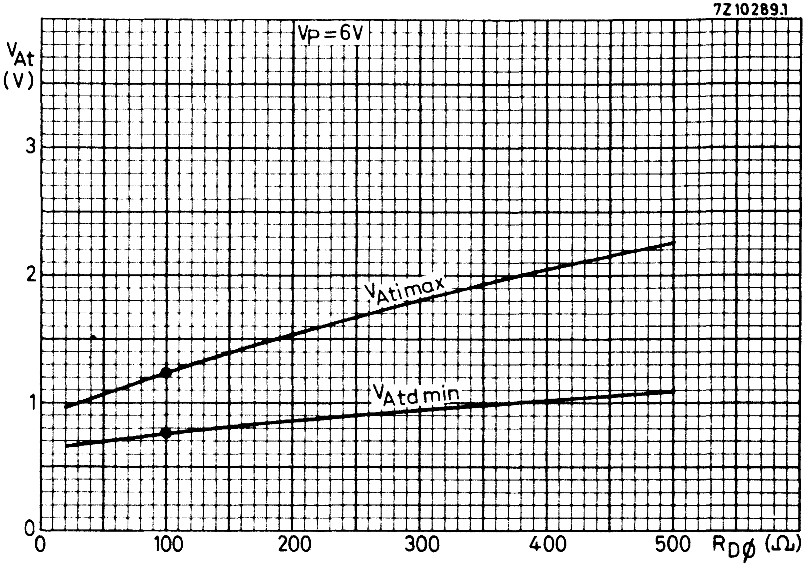
[1]) For negative output voltage.

[2]) Input voltage typ. −9 V when D grounded; no input current protection required for input voltages down to −5 V.

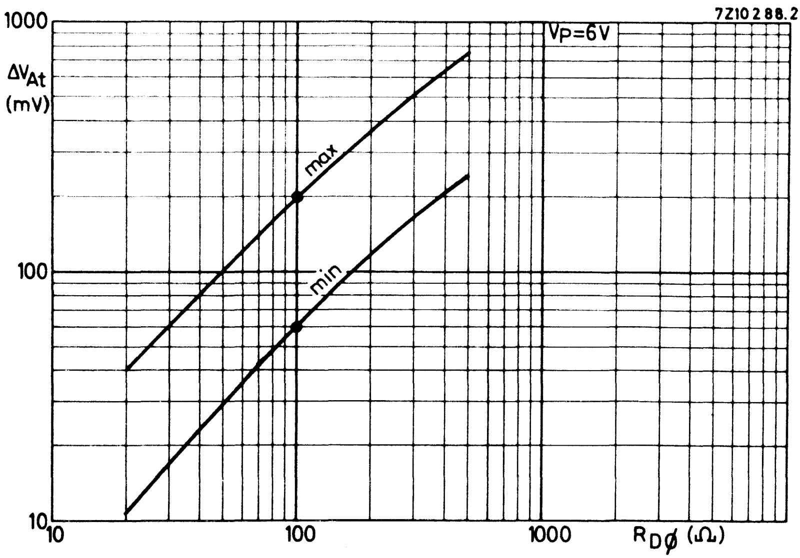
CHARACTERISTICS

		T_{amb} (°C) 0	+25	+75		Conditions and references V_P(V)	$R_{DØ}$(Ω)	
STATIC DATA								
Tripping levels								
- input voltage increasing	V_{Atimax}	1.40	1.25	1.15	V	6.0	100 ± 1%	
- input voltage decreasing	V_{Atdmin}	0.75	0.75	0.60	V	6.0	100 ± 1%	
Input hysteresis voltage	ΔV_{Atmin}	60	60	50	mV	6.0	100 ± 1%	
	ΔV_{Atmax}	220	200	180	mV	6.0	100 ± 1%	
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	0	
at: Output current LOW	I_{QLmax}	10	10	7	mA			
and at: Input voltage LOW	V_{ALmax}	0.60	0.60	0.45	V			
Output voltage LOW	V_{QLmax}	0.8	0.8	0.8	V	5.7 and 6.3	100 ± 1%	$V_{ALmax} = V_{Atd\,min}$
at: Output current LOW	I_{QLmax}	2.5	2.9	1.9	mA	5.7		
		2.1	2.5	1.6	mA	6.3		
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7	0	$I_Q = 0$
at: Input voltage HIGH	V_{AHmin}	0.95	0.90	0.80	V			
Input current HIGH	I_{AHmax}	2.2	2.0	2.0	mA	5.7 and 6.3	0	$V_A = 2\,V$
Input current HIGH	I_{AHmax}	1.2	1.1	1.2	mA	5.7 and 6.3	100 ± 1%	$V_A = 2\,V$
Output current LOW	$-I_{QLLmin}$	1.0	0.95	0.75	mA	5.7	0	$V_A = 2\,V$, V_Q externally forced to 0 V.
	$-I_{QLLmax}$	2.5	2.1	2.0	mA	6.3	0	
Supply current								
- output LOW	I_{PLmax}	4.2	3.7	3.5	mA	6.3	0	$V_A = 0\,V$
- output HIGH	I_{PHmax}	2.9	2.6	2.5	mA	6.3	0	$V_A = 2\,V$
DYNAMIC DATA								
Operating frequency	f_{min}	–	1	–	MHz	6.0	100 ± 1%	
	f_{typ}	–	5	–	MHz			

DESIGN CURVES at T_{amb} = 25 °C (dots indicate guaranteed values)

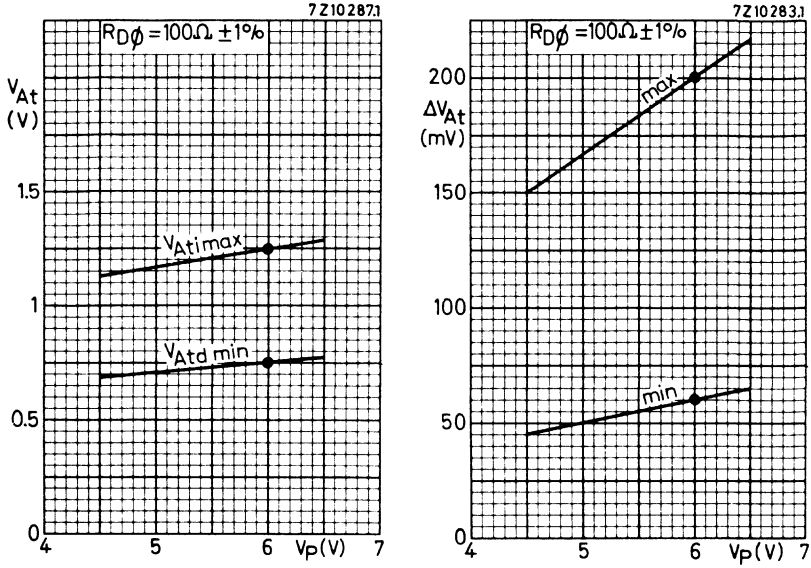


Input tripping levels versus feedback resistance

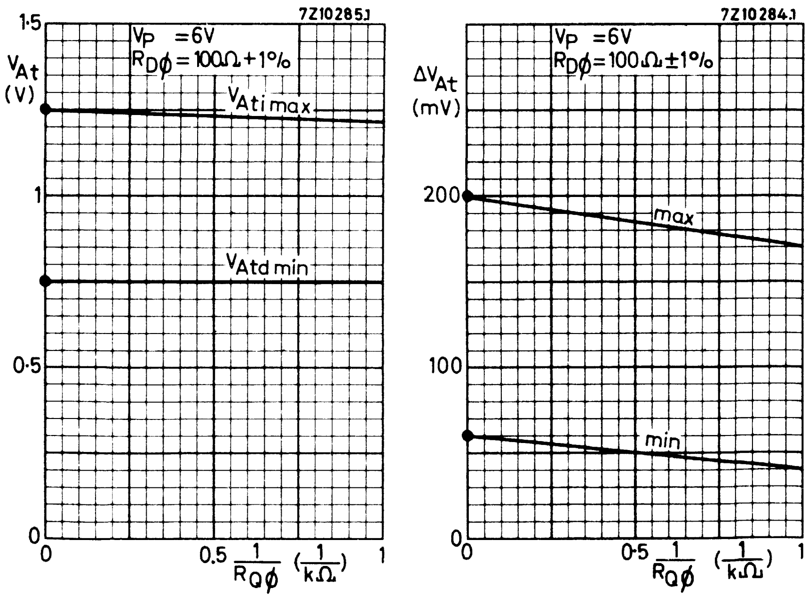


Input hysteresis voltage versus feedback resistance

DESIGN CURVES (continued) at T_{amb} = 25 °C

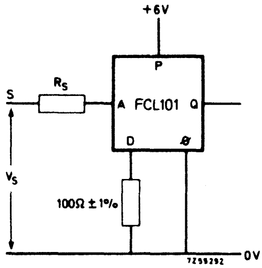


Input tripping levels and hysteresis voltage versus supply voltage

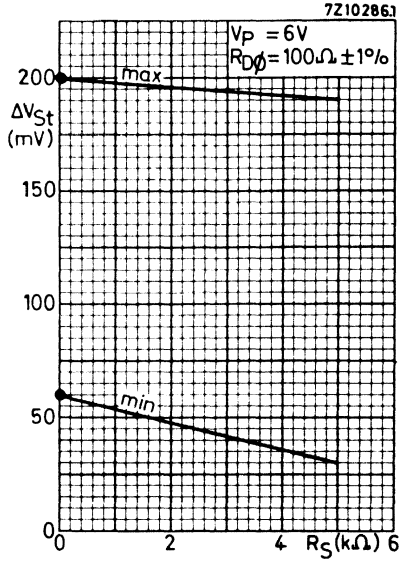


Input tripping levels and hysteresis voltage versus load conductance

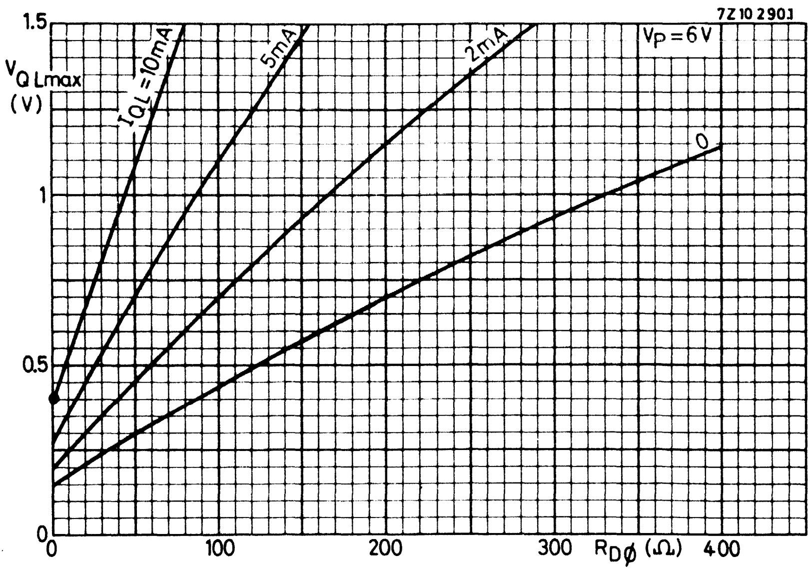
DESIGN CURVES (continued) at T_{amb} = 25 °C



ΔV_{St} = hysteresis at point S.



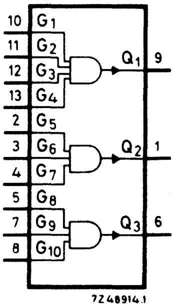
Hysteresis at signal source versus resistance

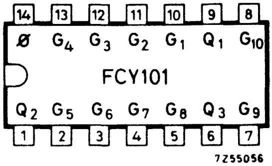


Low output voltage versus feedback resistance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

TRIPLE GATE EXPANDER





CHARACTERISTICS

			Tamb (°C) 25	75	
Reverse breakdown voltage at I_R = 50 μA	$V_{(BR)R}$	min.	8.0		V
Reverse leakage current at V_R = 8.0 V	I_R	max.	1.0	25	μA
Forward voltage at I_F = 2.0 mA	V_F	max.	1.0		V
Capacitance at V_R = 0; f = 1 MHz	C_d	max.	11		pF
Reverse recovery time at I_F = I_R = 2.0 mA	t_{rr}	typ.	4		ns
		max.	11		ns

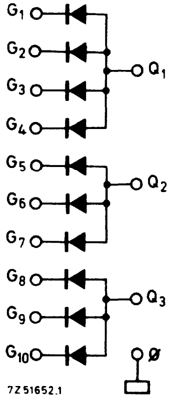
The FCY101 comprises three independent diode arrays. It is intended primarily for expanding the fan-in capability of those FCH gates that have an expansion input terminal.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Reverse voltage	V_R	max.	8.0	V
Forward current	I_F	max.	30	mA
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



CML GX family

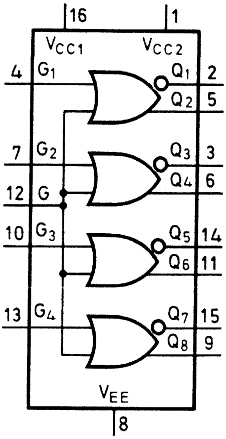
GXB10101	quadruple OR/NOR gate
GXB10102	quadruple NOR gate
GXB10105	triple OR/NORgate
GXB10106	triple NOR gate
GXB10107	triple EXCLUSIVE OR/EXCLUSIVE NOR gate
GXB10109	dual OR/NOR gate
GXB10110	dual 3-input/3-output OR line driver
GXB10111	dual 3-input/3-output NOR line driver
GXB10115	quadruple line receiver
GXB10117	dual OR-AND/OR-AND-INVERT gate
GXB10118	dual OR/AND gate
GXB10119	OR/AND gate
GXB10121	4-wide OR-AND/OR-AND-INVERT gate
GXB10130	dual D-LATCH
GXB10131	dual D-type master-slave FLIP-FLOP
GXB10160	12-bit PARITY CHECKER/GENERATOR
GXB10161	three-bit DECODER (one of eight lines LOW)
GXB10162	three-bit DECODER (one of eight lines HIGH)
GXB10164	eight input MULTIPLEXER

The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

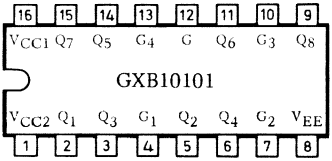
The GXB10101 is a quadruple 2-input OR/NOR gate with one input from each gate common to pin 12.

Input pull-down resistors (50 kΩ) allow unused inputs to be left open.
The GX family corresponds to the ECL10000 series.

QUADRUPLE OR/NOR GATE



7Z67176

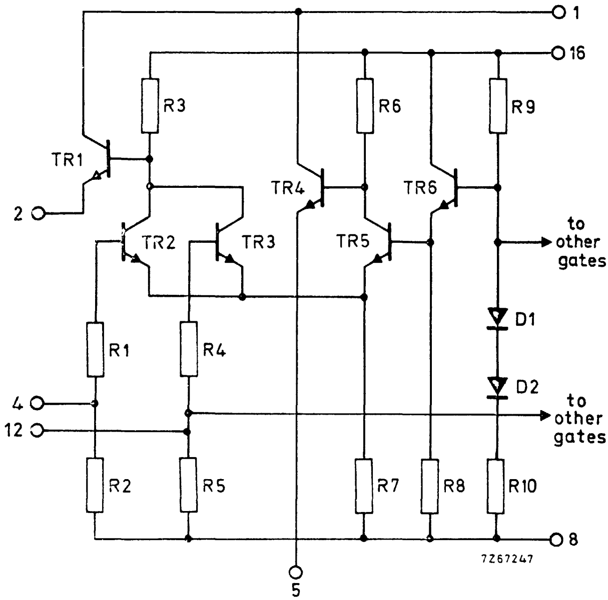


$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5,2$ V

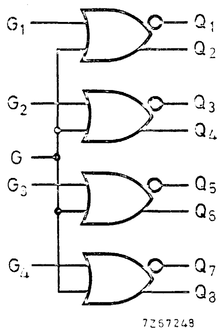
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	2,0	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	100	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM (one gate)



LOGIC FUNCTION



$Q_1 = \overline{G_1 + G}$ $Q_5 = \overline{G_3 + G}$

$Q_2 = G_1 + G$ $Q_6 = G_3 + G$

$Q_3 = \overline{G_2 + G}$ $Q_7 = \overline{G_4 + G}$

$Q_4 = G_2 + G$ $Q_8 = G_4 + G$

positive logic: HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

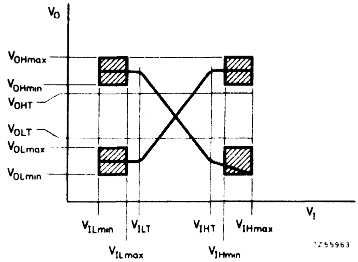
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = -5,2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0,840	−0,810	−0,720	V
V_{IHT}	−1,145	−1,105	−1,045	V
V_{ILT}	−1,490	−1,475	−1,450	V
V_{ILmin}	−1,870	−1,850	−1,830	V

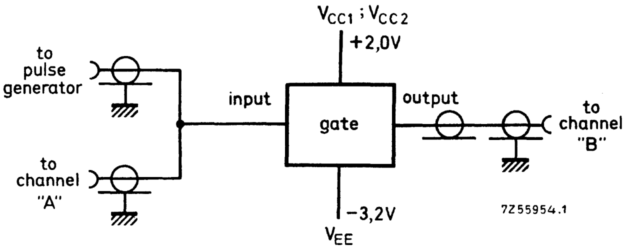


	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	−1000	−960	−900	mV	$V_{IL\,min}$ on inputs for invert outputs $V_{IH\,max}$ on inputs for direct outputs
		typ.	-	−880	-	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1,870	−1,850	−1,830	V	$V_{IH\,max}$ on inputs for invert outputs $V_{IL\,min}$ on inputs for direct outputs
		typ.	-	−1,720	-	V	
		max.	−1,665	−1,650	−1,625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	V_{ILT} on one input for invert outputs V_{IHT} on one input for direct outputs
Output threshold voltage LOW	V_{OLT}	max.	−1,645	−1,630	−1,605	V	one input at V_{ILT} or V_{IHT}
Input current HIGH	I_{IH} pin 12	max.	-	500	-	μA	$V_{IH\,max}$ for input under test
	I_{IH} other inputs	max.	-	265	-	μA	
Input current LOW	I_{IL}	min.	-	10	-	μA	$V_{IL\,min}$ for input under test
Supply current	I_{EE}	typ.	-	20	-	mA	$V_{IL\,min}$ for all inputs
		max.	-	26	-	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	-	0,25	-		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C.

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay times:						
OR output	t_{pdrOR}	1,0	2,0	2,9	ns	See waveforms on page 5
NOR output	t_{pdrNOR}	1,0	2,0	2,9	ns	
Fall propagation delay times:						
OR output	t_{pdfOR}	1,0	2,0	2,9	ns	
NOR output	t_{pdfNOR}	1,0	2,0	2,9	ns	
Rise time	t_r	1,1	2,0	3,3	ns	
Fall time	t_f	1,1	2,0	3,3	ns	
Input capacitance (see note 1)	C_I pin 12	-	-	10	pF	reflection measurement
	C_I other inputs	-	-	5	pF	

Switching times test circuit

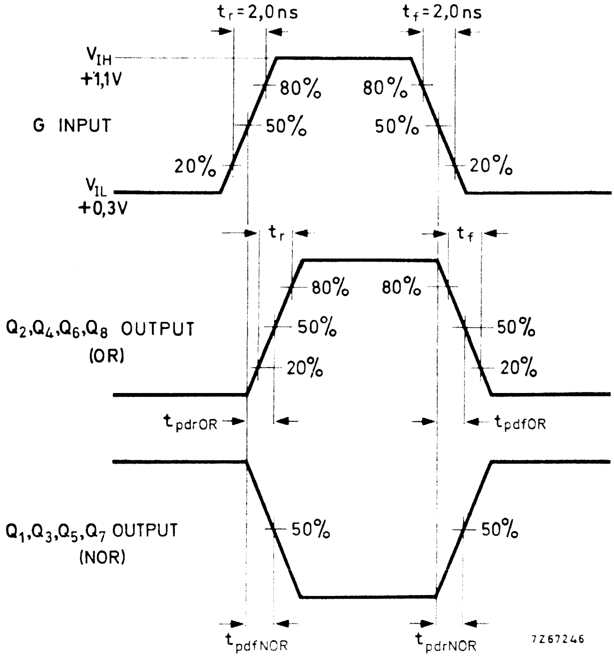


Notes

1. Input resistance is positive at any frequency.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

Switching times waveforms

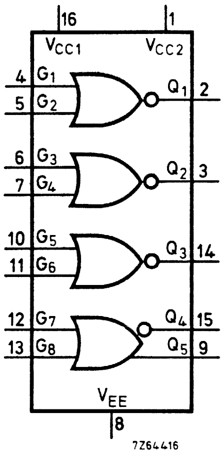


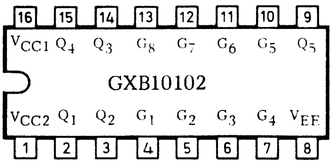
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10102 is a quadruple 2-input NOR gate.

Input pull-down resistors (50 kΩ) allow unused inputs to be left open.
The GX family corresponds to the ECL10 000series.

QUADRUPLE NOR GATE



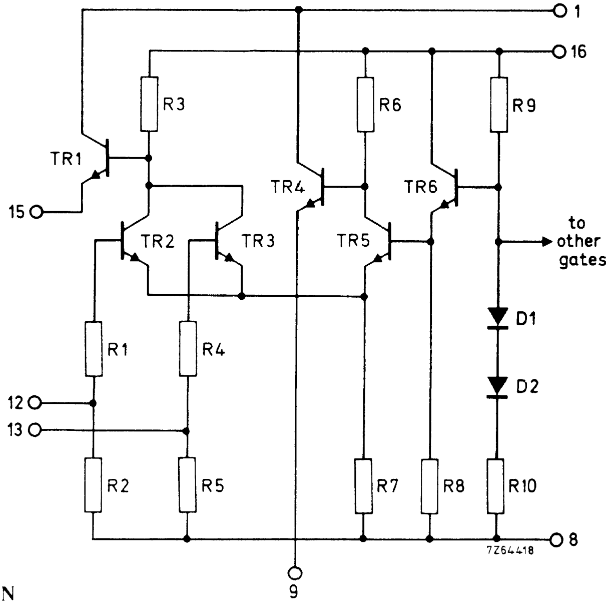


$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5,2$ V

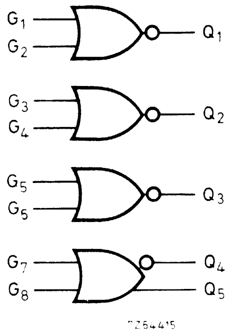
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		−5, 2 ± 10%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	2, 0	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	100	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM (one gate)



LOGIC FUNCTION



$Q_1 = \overline{G_1 + G_2}$

$Q_2 = \overline{G_3 + G_4}$

$Q_3 = \overline{G_5 + G_6}$

$Q_4 = \overline{G_7 + G_8}$

$Q_5 = \overline{Q_4}$

positive logic: HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

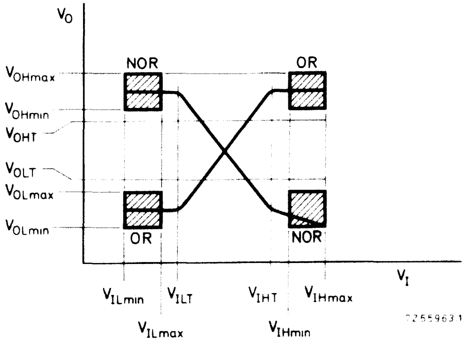
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2, 5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2, 0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0, 840	−0, 810	−0, 720	V
V_{IHT}	−1, 145	−1, 105	−1, 045	V
V_{ILT}	−1, 490	−1, 475	−1, 450	V
V_{ILmin}	−1, 870	−1, 850	−1, 830	V

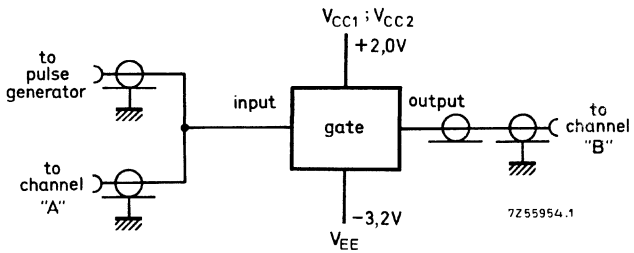


	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min	−1000	−960	−900	mV	V_{ILmin} on inputs for invert outputs V_{IHmax} on inputs 12; 13 for output 9
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1, 870	−1, 850	−1, 830	V	V_{IHmax} on inputs for invert outputs V_{ILmin} on inputs 12; 13 for output 9
		typ.	−	−1, 720	−	V	
		max.	−1, 665	−1, 650	−1, 625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	V_{ILT} on one input for invert outputs V_{IHT} on input 12 or 13 for output 9
Output threshold voltage LOW	V_{OLT}	max.	−1, 645	−1, 630	−1, 605	V	one input at V_{ILT} or V_{IHT}
Input current HIGH	I_{IH}	max.	−	265	−	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	20	−	mA	V_{ILmin} for all inputs
		max.	−	26	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0, 25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time; OR output	t_{pdrOR}	1,0	2,0	2,9	ns	See waveforms on page 5
Fall propagation delay time; OR output	t_{pdfOR}	1,0	2,0	2,9	ns	
Rise propagation delay time; NOR output	t_{pdrNOR}	1,0	2,0	2,9	ns	
Fall propagation delay time; NOR output	t_{pdfNOR}	1,0	2,0	2,9	ns	
Rise time	t_r	1,1	2,0	3,3	ns	
Fall time	t_f	1,1	2,0	3,3	ns	
Input capacitance (see note 1)	C_I	–	–	5	pF	reflection measurement

Switching times test circuit

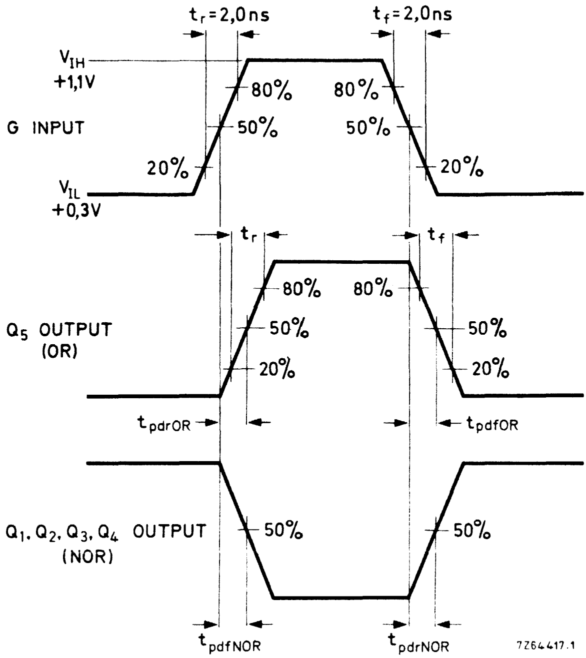


Notes

1. Input resistance is positive at any frequency.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

Switching times waveforms

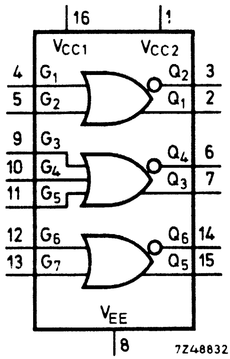


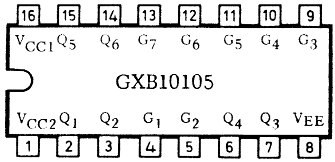
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10105 is a triple 2-3-2 input OR/NOR gate.

Input pull-down resistors (50 kΩ) allow unused inputs to be left open.
The GX family corresponds to the ECL10 000series.

TRIPLE OR/NOR GATE



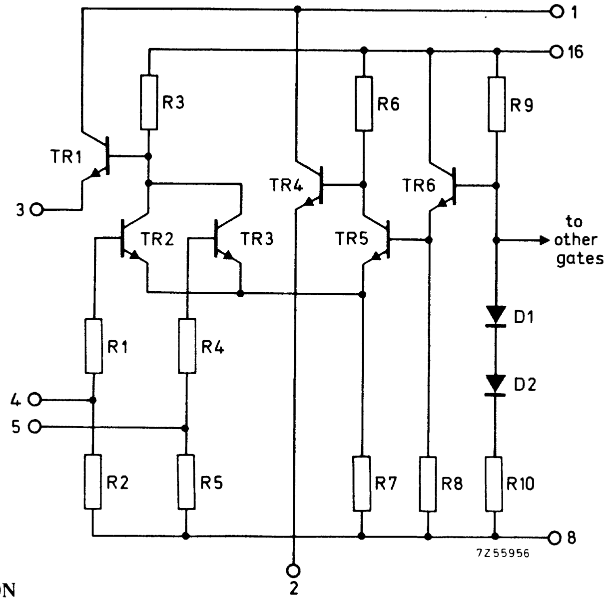


$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5,2$ V

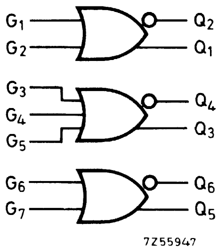
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	2,0	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	75	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM (one gate)



LOGIC FUNCTION



$Q_1 = G_1 + G_2$ $\quad$ $Q_2 = \overline{G_1 + G_2}$

$Q_3 = G_3 + G_4 + G_5$ $\quad$ $Q_4 = \overline{G_3 + G_4 + G_5}$

$Q_5 = G_6 + G_7$ $\quad$ $Q_6 = \overline{G_6 + G_7}$

positive logic: HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

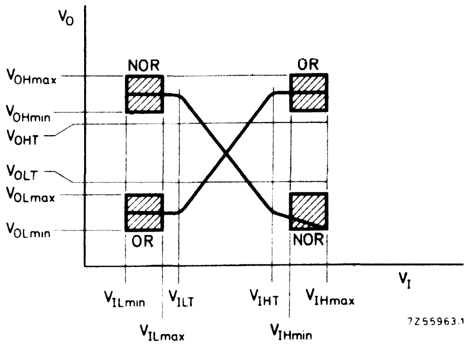
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2, 5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2, 0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0, 840	−0, 810	−0, 720	V
V_{IHT}	−1, 145	−1, 105	−1, 045	V
V_{ILT}	−1, 490	−1, 475	−1, 450	V
V_{ILmin}	−1, 870	−1, 850	−1, 830	V

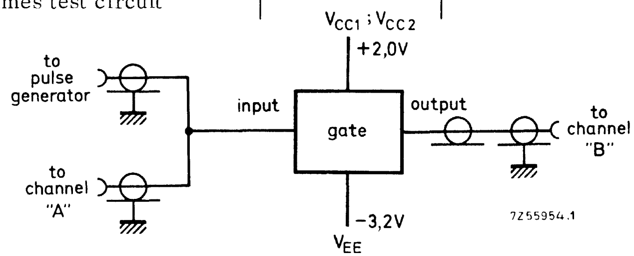


	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min typ. max.	−1000 − −840	−960 −880 −810	−900 − −720	mV mV mV	V_{IHmax} or V_{ILmin}
Output voltage LOW	V_{OL}	min. typ. max.	−1, 870 − −1, 665	−1, 850 −1, 720 −1, 650	−1, 830 − −1, 625	V V V	V_{ILmin} or V_{IHmax}
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	one input at V_{IHT} or V_{ILT}
Output threshold voltage LOW	V_{OLT}	max.	−1, 645	−1, 630	−1, 605	V	one input at V_{ILT} or V_{IHT}
Input current HIGH	I_{IH}	max.	−	265	−	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ. max.	− −	15 21	− −	mA mA	V_{ILmin} for all inputs
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0, 25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5, 2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time; OR output	t_{pdrOR}	1, 0	2, 0	2, 9	ns	See waveforms on page 5
Fall propagation delay time; OR output	t_{pdfOR}	1, 0	2, 0	2, 9	ns	See waveforms on page 5
Rise propagation delay time; NOR output	t_{pdrNOR}	1, 0	2, 0	2, 9	ns	See waveforms on page 5
Fall propagation delay time; NOR output	t_{pdfNOR}	1, 0	2, 0	2, 9	ns	See waveforms on page 5
Rise time	t_r	1, 1	2, 0	3, 3	ns	See waveforms on page 5
Fall time	t_f	1, 1	2, 0	3, 3	ns	See waveforms on page 5
Input capacitance (see note 1)	C_I	−	−	5	pF	reflection measurement

Switching times test circuit

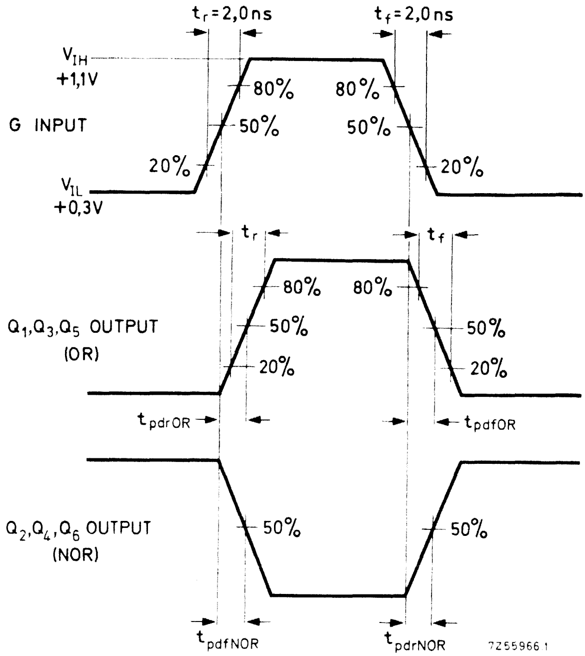


Notes

1. Input resistance is positive at any frequency.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

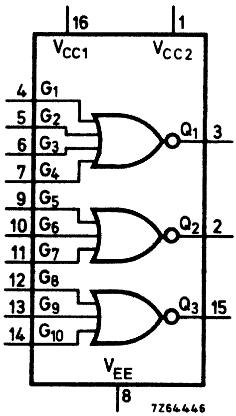
Switching times waveforms

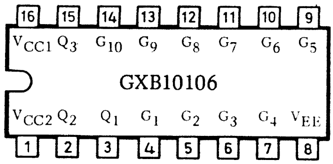


The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.
The GXB10106 is a triple 4-3-3 input NOR gate.

Input pull-down resistors (50 kΩ) allow unused inputs to be left open.
The GX family corresponds to the ECL10 000 series.

TRIPLE NOR GATE





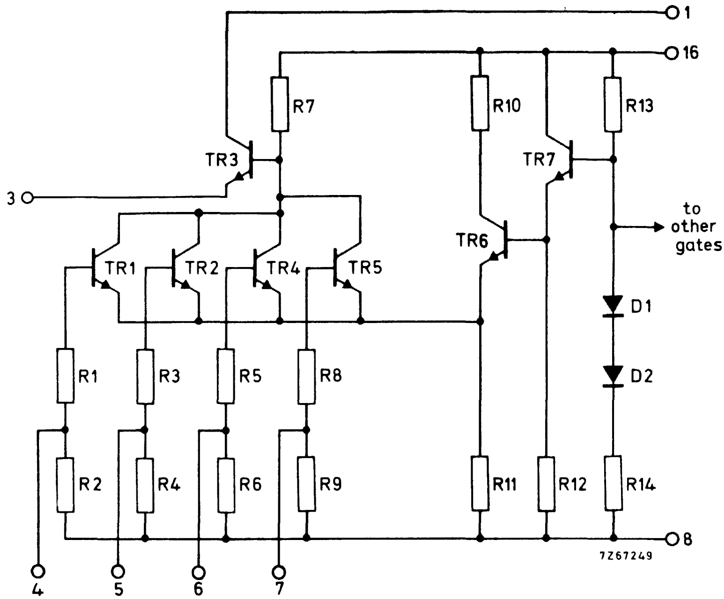
V_{CC1} = V_{CC2} = 0 V (ground)
V_{EE} = −5, 2 V

QUICK REFERENCE DATA

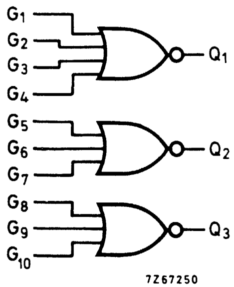
Supply voltage	V_{EE}		−5, 2 ± 10%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	2, 0	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	75	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM (one gate)



LOGIC FUNCTION



$Q_1 = \overline{G_1 + G_2 + G_3 + G_4}$

$Q_2 = \overline{G_5 + G_6 + G_7}$

$Q_3 = \overline{G_8 + G_9 + G_{10}}$

positive logic: HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

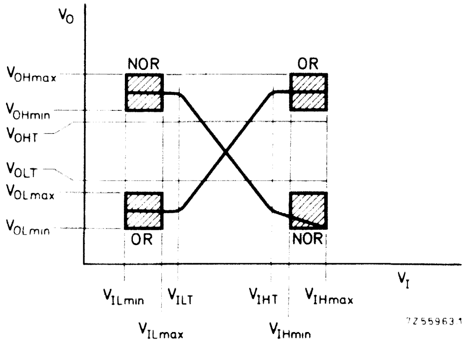
Supply voltage d.c.	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5,2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0,840	−0,810	−0,720	V
V_{IHT}	−1,145	−1,105	−1,045	V
V_{ILT}	−1,490	−1,475	−1,450	V
V_{ILmin}	−1,870	−1,850	−1,830	V

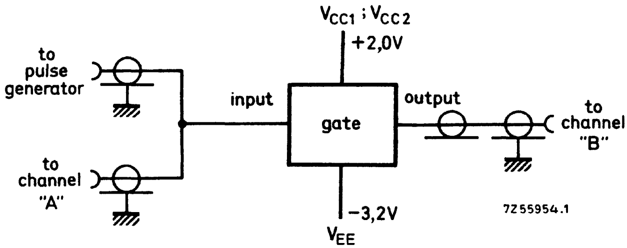


	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	−1000	−960	−900	mV	one input at V_{ILmin}
		typ.	–	−880	–	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW		min.	−1,870	−1,850	−1,830	V	one input at V_{IHmax}
		typ.	–	−1,720	–	V	
		max.	−1,665	−1,650	−1,625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	one input at V_{ILT}
Output threshold voltage LOW	V_{OLT}	max.	−1,645	−1,630	−1,605	V	one input at V_{IHT}
Input current HIGH	I_{IH}	max.	–	265	–	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}	min.	–	10	–	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	–	15	–	mA	V_{ILmin} for all inputs
		max.	–	21	–	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	–	0,25	–		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time; NOR output	t_{pdrNOR}	1,0	2,0	2,9	ns	See waveforms on page 5
Fall propagation delay time; NOR output	t_{pdfNOR}	1,0	2,0	2,9	ns	
Rise time	t_r	1,1	2,0	3,3	ns	
Fall time	t_f	1,1	2,0	3,3	ns	
Input capacitance (see note 1)	C_I	–	–	5	pF	reflection measurement

Switching times test circuit

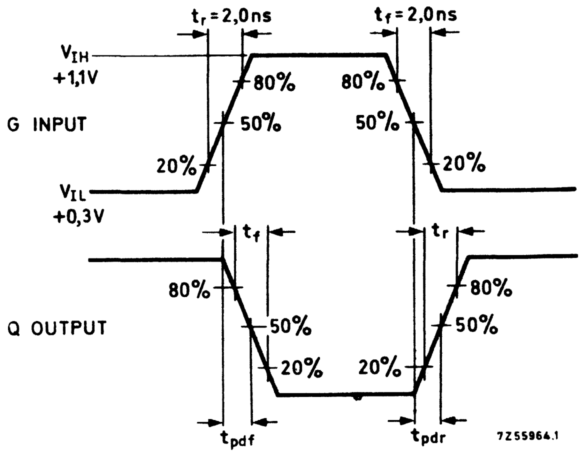


Notes

1. Input resistance is positive at any frequency.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

Switching times waveforms



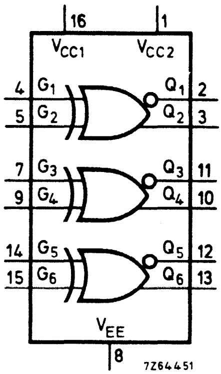
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

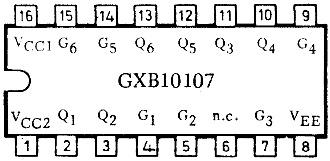
The GXB10107 is a three gate array designed to provide the positive EXCLUSIVE OR and NOR functions.

Input pull-down resistors (50 kΩ) allow unused inputs to be left open.

The GX family corresponds to the ECL10 000series.

TRIPLE EXCLUSIVE OR/EXCLUSIVE NOR GATE



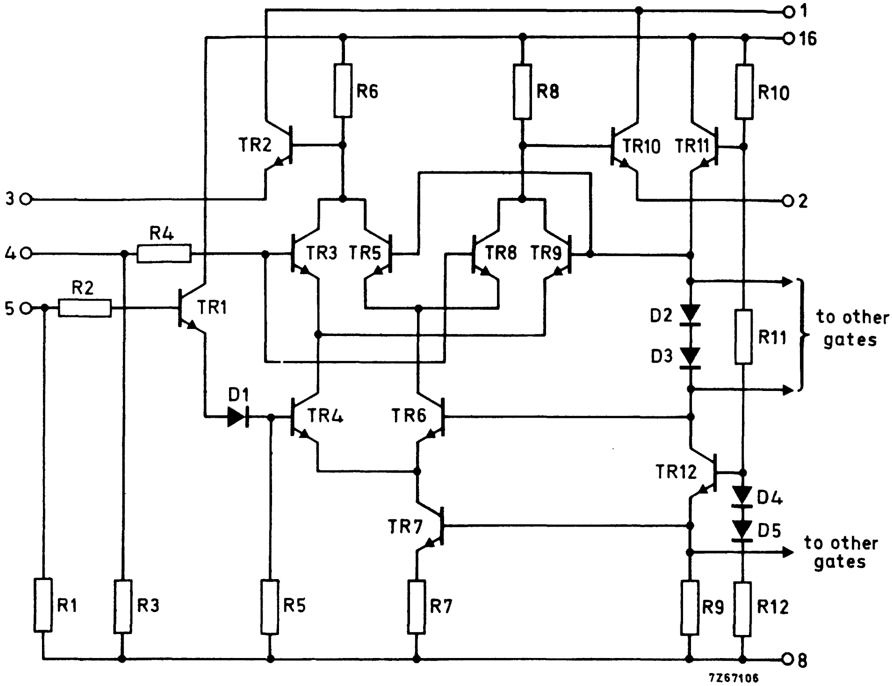


$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5,2$ V

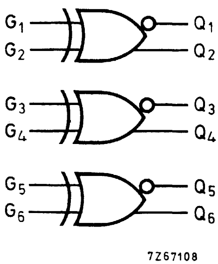
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		$-5,2 \pm 10\%$	V
Operating ambient temperature	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	2,4	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	115	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM (one gate)



LOGIC FUNCTION



$Q_1 = \overline{G_1} \cdot \overline{G_2} + G_1 \cdot G_2$

$Q_2 = G_1 \cdot \overline{G_2} + \overline{G_1} \cdot G_2$

$Q_3 = \overline{G_3} \cdot \overline{G_4} + G_3 \cdot G_4$

$Q_4 = G_3 \cdot \overline{G_4} + \overline{G_3} \cdot G_4$

$Q_5 = \overline{G_5} \cdot \overline{G_6} + G_5 \cdot G_6$

$Q_6 = G_5 \cdot \overline{G_6} + \overline{G_5} \cdot G_6$

positive logic: HIGH state = 1
LOW state = 0

RATINGS Limitng values in accordance with the Absolute Maximum System (IEC 134)

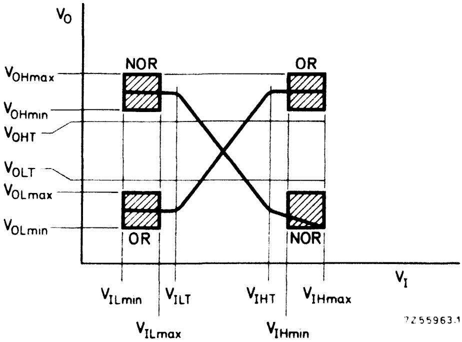
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	^oC
Junction temperature	T_j	max.	125	^oC

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5,2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	-0, 840	-0, 810	-0, 720	V
V_{IHT}	-1, 145	-1, 105	-1, 045	V
V_{ILT}	-1, 490	-1, 475	-1, 450	V
V_{ILmin}	-1, 870	-1, 850	-1, 830	V



	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	-1000	-960	-900	mV	See note 1
		typ.	–	-880	–	mV	
		max.	-840	-810	-720	mV	
Output voltage LOW	V_{OL}	min.	-1,870	-1,850	-1,830	V	See note 2
		typ.	-	-1,720	–	V	
		max.	-1,665	-1,650	-1,625	V	
Output threshold voltage HIGH	V_{OHT}	min.	-1020	-980	-920	mV	See note 3
Output threshold voltage LOW	V_{OLT}	max.	-1,645	-1,630	-1 ,605	V	See note 4

Notes

1. V_{ILmin} or V_{IHmax} on both inputs for invert outputs.
   V_{ILmin} on one input and V_{IHmax} on other input for direct outputs.
2. V_{ILmin} on one input and V_{IHmax} on other input for invert outputs.
   V_{ILmin} or V_{IHmax} on both inputs for direct outputs.
3. V_{ILT} or V_{IHT} on both inputs for invert outputs.
   V_{ILT} on one input and V_{IHT} on other input for direct outputs.
4. V_{ILT} on one input and V_{IHT} on other input for invert outputs.
   V_{ILT} or V_{IHT} on both inputs for direct outputs.

CHARACTERISTICS (continued)

	Symbol		T_{amb} (°C) 0	25	75		Conditions
Input current HIGH							
pins 4, 9, 14	I_{IH}	max.	–	350	–	μA	V_{IHmax} for input under test
pins 5, 7, 15	I_{IH}	max.	–	265	–	μA	
Input current LOW	I_{IL}	min.	–	10	–	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	–	23	–	mA	V_{IHmax} for all inputs
		max.	–	28	–	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	–	0, 25	–		

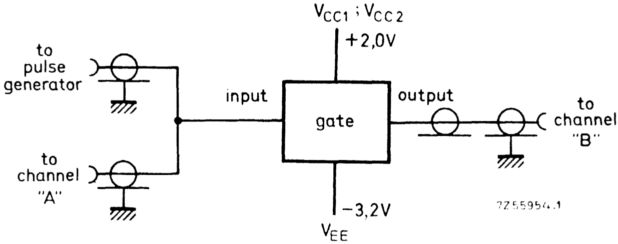
CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = –5, 2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay times:						
OR output	t_{pdrOR}	1, 1	2, 0	3, 7	ns	Inputs 4, 9 or 14
		1, 1	2, 8	3, 7	ns	Inputs 5, 7 or 15
NOR output	t_{pdrNOR}	1, 1	2, 0	3, 7	ns	Inputs 4, 9 or 14
		1, 1	2, 8	3, 7	ns	Inputs 5, 7 or 15
Fall propagation delay times:						
OR output	t_{pdfOR}	1, 1	2, 0	3, 7	ns	Inputs 4, 9 or 14
		1, 1	2, 8	3, 7	ns	Inputs 5, 7 or 15
NOR output	t_{pdfNOR}	1, 1	2, 0	3, 7	ns	Inputs 4, 9 or 14
		1, 1	2, 8	3, 7	ns	Inputs 5, 7 or 15
Rise time	t_r	1, 1	2, 5	3, 5	ns	
Fall time	t_f	1, 1	2, 5	3, 5	ns	
Input capacitance (see note)	C_I	–	-	5	pF	reflection measurement

Note: Input resistance is positive at any frequency

CHARACTERISTICS (continued)

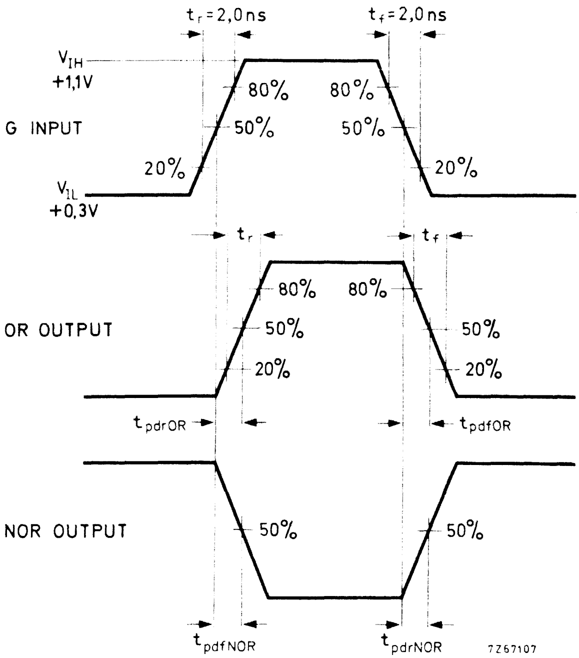
Switching times test circuit



Notes

1. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
2. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.
3. Input impedance of the oscilloscope is 50 Ω.

Switching times waveforms

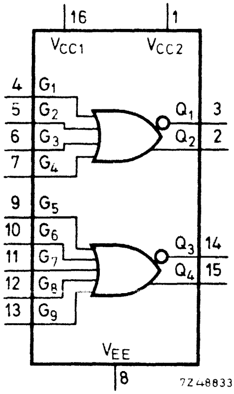


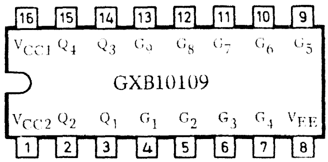
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10109 is a dual 4-5 input OR/NOR gate.

Input pull-down resistors (50 kΩ) allow unused inputs to be left open.
The GX family corresponds to the ECL10 000series.

DUAL OR/NOR GATE



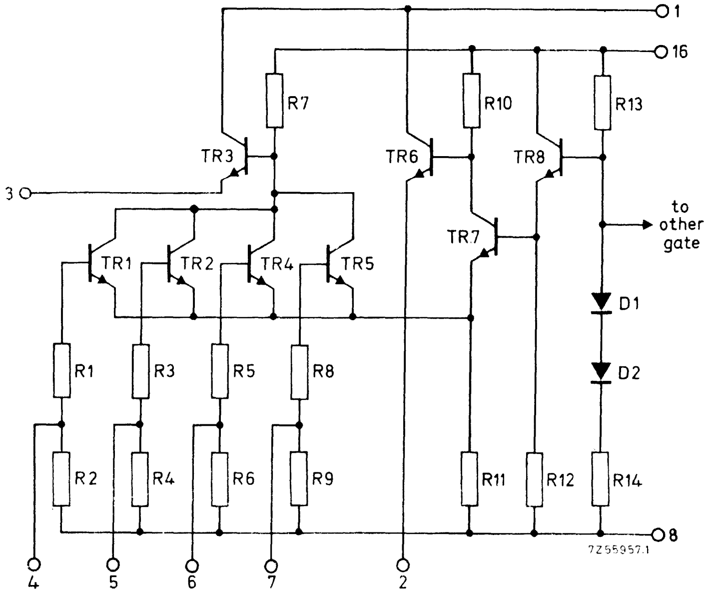


$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5,2$ V

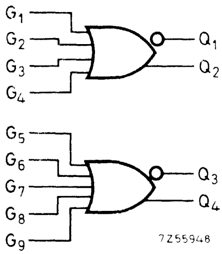
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		$-5,2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	2,0	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	50	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM (one gate)



LOGIC FUNCTION



$$Q_1 = \overline{G_1 + G_2 + G_3 + G_4}$$

$$Q_3 = \overline{G_5 + G_6 + G_7 + G_8 + G_9}$$

$$Q_2 = G_1 + G_2 + G_3 + G_4$$

$$Q_4 = G_5 + G_6 + G_7 + G_8 + G_9$$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

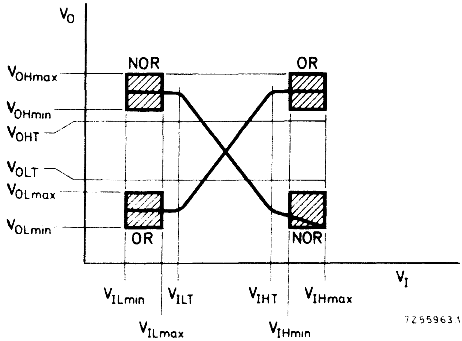
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2, 5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2, 0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0, 840	−0, 810	−0, 720	V
V_{IHT}	−1, 145	−1, 105	−1, 045	V
V_{ILT}	−1, 490	−1, 475	−1, 450	V
V_{ILmin}	−1, 870	−1, 850	−1, 830	V

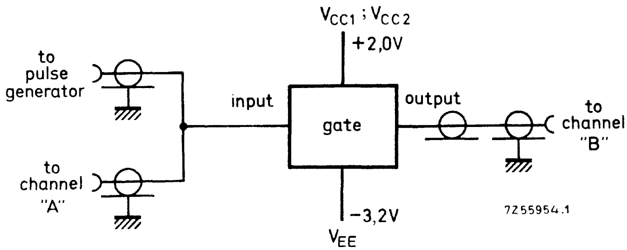


	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min	−1000	−960	−900	mV	V_{IHmax} or V_{ILmin}
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1, 870	−1, 850	−1, 830	V	V_{ILmin} or V_{IHmax}
		typ.	−	−1, 720	−	V	
		max.	−1, 665	−1, 650	−1, 625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	V_{IHT} or V_{ILT}
Output threshold voltage LOW	V_{OLT}	max.	−1, 645	−1, 630	−1, 605	V	V_{ILT} or V_{IHT}
Input current HIGH	I_{IH}	max.	−	265	−	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	10	−	mA	V_{ILmin} for all inputs
		max.	−	14	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0, 25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time; OR output	t_{pdrOR}	1,0	2,0	2,9	ns	See waveforms on page 5
Fall propagation delay time; OR output	t_{pdfOR}	1,0	2,0	2,9	ns	
Rise propagation delay time; NOR output	t_{pdrNOR}	1,0	2,0	2,9	ns	
Fall propagation delay time; NOR output	t_{pdfNOR}	1,0	2,0	2,9	ns	
Rise time	t_r	1,1	2,0	3,3	ns	
Fall time	t_f	1,1	2,0	3,3	ns	
Input capacitance (see note 1)	C_I	–	–	5	pF	reflection measurement

Switching times test circuit

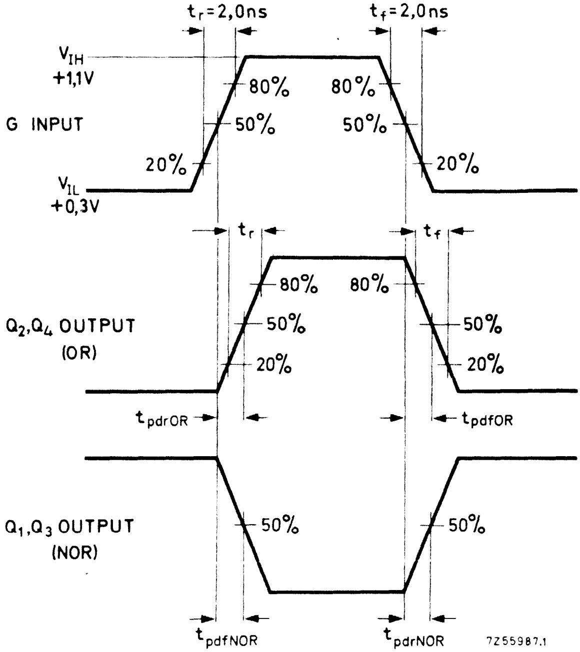


Notes

1. Input resistance is positive at any frequency.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests..

CHARACTERISTICS (continued)

Switching times waveforms

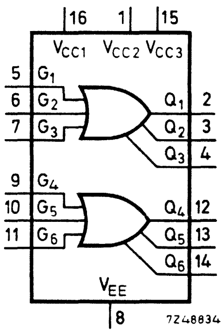


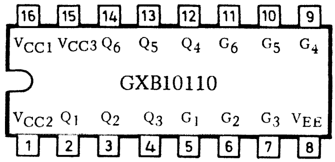
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10110 is a dual 3-input/3-output OR gate intended to drive up to three transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications.

The GX family corresponds to the ECL10 000series.

DUAL 3-INPUT/3-OUTPUT OR LINE DRIVER



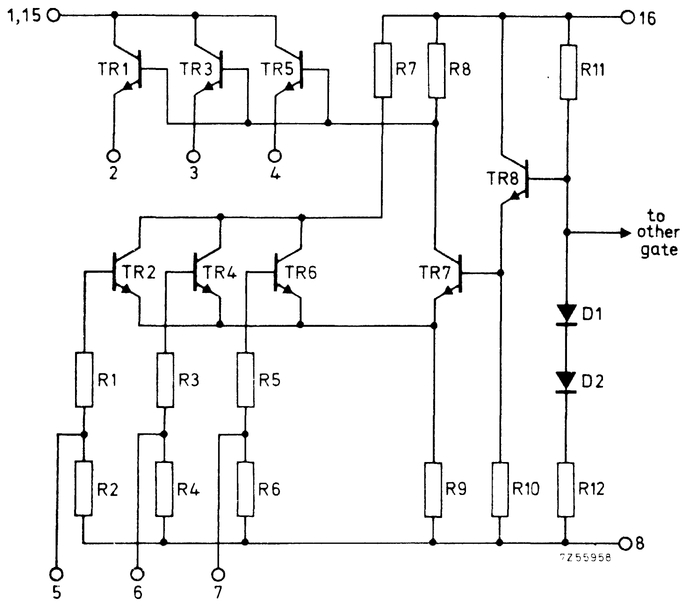


$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground)
$V_{EE} = -5,2$ V

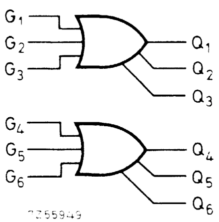
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		−5, 2 ± 10%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	2, 4	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	150	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM (one gate)



LOGIC FUNCTION



$Q_1 = Q_2 = Q_3 = G_1 + G_2 + G_3$

$Q_4 = Q_5 = Q_6 = G_4 + G_5 + G_6$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

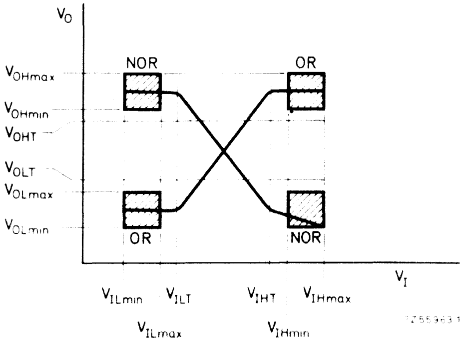
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5,2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0,840	−0,810	−0,720	V
V_{IHT}	−1,145	−1,105	−1,045	V
V_{ILT}	−1,490	−1,475	−1,450	V
V_{ILmin}	−1,870	−1,850	−1,830	V

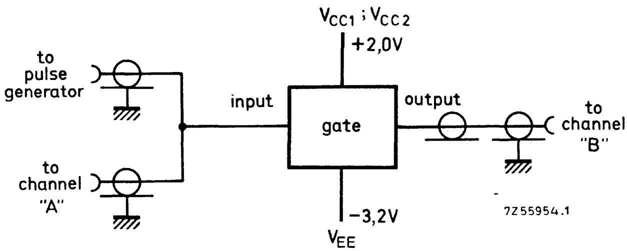


	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min	−1000	−960	−900	mV	one input at V_{IHmax}
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1,870	−1,850	−1,830	V	one input at V_{ILmin}
		typ.	−	−1,720	−	V	
		max.	−1,665	−1,650	−1,625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	one input at V_{IHT}
Output threshold voltage LOW	V_{OLT}	max.	−1,645	−1,630	−1,605	V	one input at V_{ILT}
Input current HIGH	I_{IH}	max.	−	400	−	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	30	−	mA	V_{ILmin} for all inputs
		max.	−	38	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0,25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5, 2 V ; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time; OR output	t_{pdr}	1, 4	2, 4	3, 5	ns	See waveforms on page 5
Fall propagation delay time; OR output	t_{pdf}	1, 4	2, 4	3, 5	ns	See waveforms on page 5
Rise time	t_r	1, 1	2, 0	3, 5	ns	See waveforms on page 5
Fall time	t_f	1, 1	2, 0	3, 5	ns	See waveforms on page 5
Input capacitance (see note 1)	C_I	−	−	7	pF	reflection measurement

Switching times test circuit

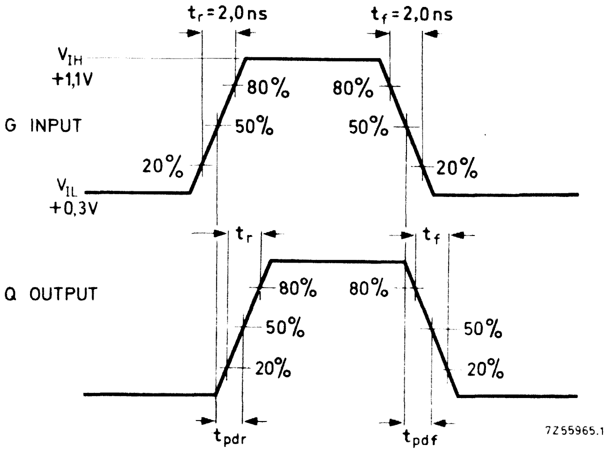


Notes

1. Input resistance is positive at any frequency.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

Switching times waveforms

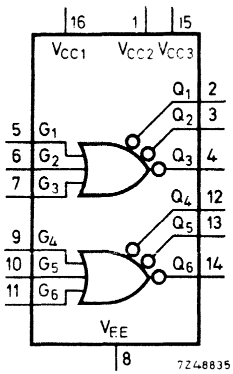


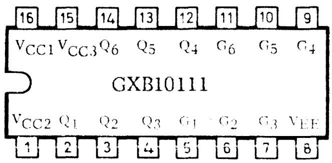
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10111 is a dual 3-input/3-output NOR gate intended to drive up to three transmission lines simultaneously. The ability to control three parallel lines makes this device particularly useful in clock distribution applications.

The GX family corresponds to the ECL10 000series.

DUAL 3-INPUT/3-OUTPUT NOR LINE DRIVER



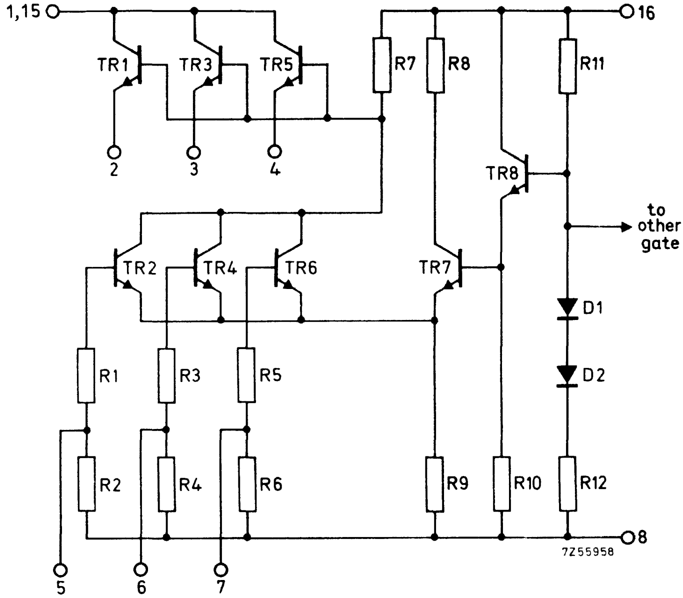


$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground)
$V_{EE} = -5,2$ V

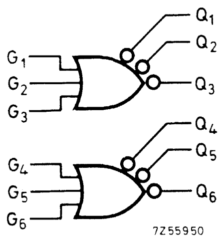
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		−5, 2 ± 10%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	2, 4	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	150	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM (one gate)



LOGIC FUNCTION



$Q_1 = Q_2 = Q_3 = \overline{G_1 + G_2 + G_3}$

$Q_4 = Q_5 = Q_6 = \overline{G_4 + G_5 + G_6}$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS Limting values in accordance with the Absolute Maximum System (IEC134)

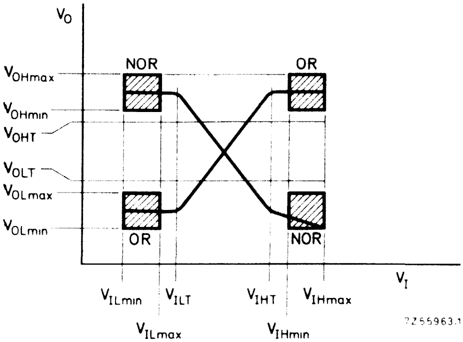
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	^oC
Junction temperature	T_j	max.	125	^oC

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2, 5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2, 0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0, 840	−0, 810	−0, 720	V
V_{IHT}	−1, 145	−1, 105	−1, 045	V
V_{ILT}	−1, 490	−1, 475	−1, 450	V
V_{ILmin}	−1, 870	−1, 850	−1, 830	V

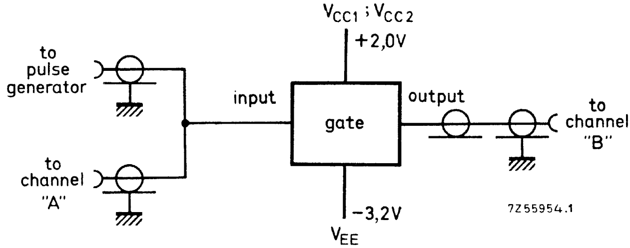


	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min	−1000	−960	−900	mV	one input at V_{ILmin}
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1, 870	−1, 850	−1, 830	V	one input at V_{IHmax}
		typ.	−	−1, 720	−	V	
		max.	−1, 665	−1, 650	−1, 625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	one input at V_{ILT}
Output threshold voltage LOW	V_{OLT}	max.	−1, 645	−1, 630	−1, 605	V	one input at V_{IHT}
Input current HIGH	I_{IH}	max.	−	400	−	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	30	−	mA	V_{ILmin} for all inputs
		max.	−	38	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0, 25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time; NOR output	t_{pdr}	1,4	2,4	3,5	ns	See waveforms on page 5
Fall propagation delay time; NOR output	t_{pdf}	1,4	2,4	3,5	ns	See waveforms on page 5
Rise time	t_r	1,1	2,1	3,5	ns	See waveforms on page 5
Fall time	t_f	1,1	2,1	3,5	ns	See waveforms on page 5
Input capacitance (see note 1)	C_I	–	–	7	pF	reflection measurement

Switching times test circuit

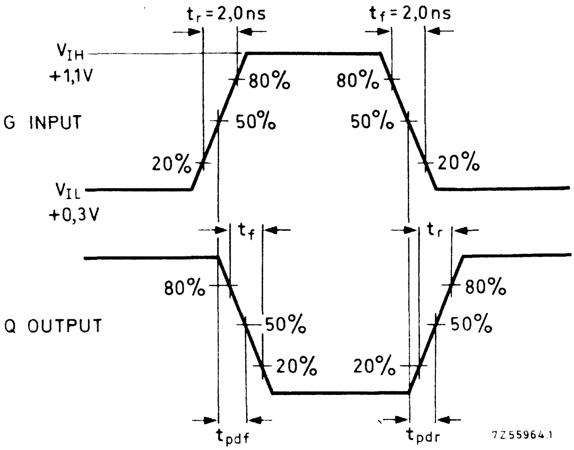


Notes

1. Input resistance is positive at any frequency.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

Switching times waveforms

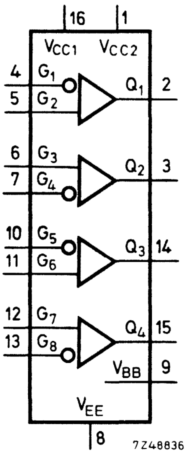


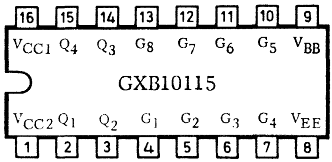
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10115 is a quadruple differential amplifier intended for use in sensing signals over long lines. The base bias supply makes the device useful in other applications where a stable reference voltage is necessary.

The GX family corresponds to the ECL10 000series.

QUADRUPLE LINE RECEIVER





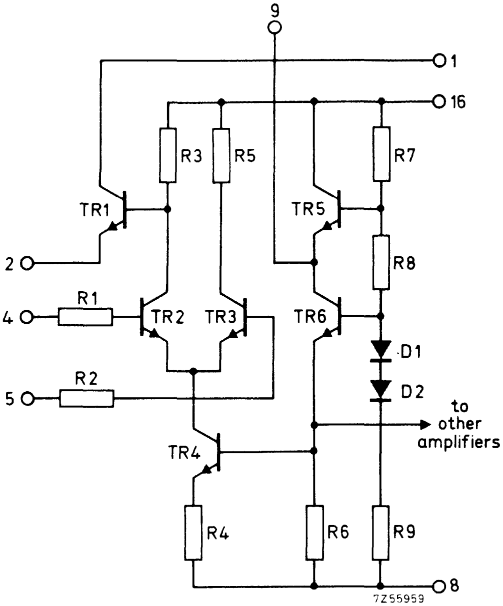
$V_{CC1} = V_{CC2} = 0$ V (ground)

$V_{EE} = -5,2$ V

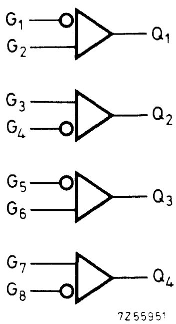
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	2,0	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	95	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM (one amplifier)



LOGIC FUNCTION



With inputs G_2, G_3, G_6, G_7 connected to V_{BB}.

$Q_1 = \overline{G_1}$ $Q_3 = \overline{G_5}$

$Q_2 = \overline{G_4}$ $Q_4 = \overline{G_8}$

Positive logic: HIGH state = 1
LOW state = 0

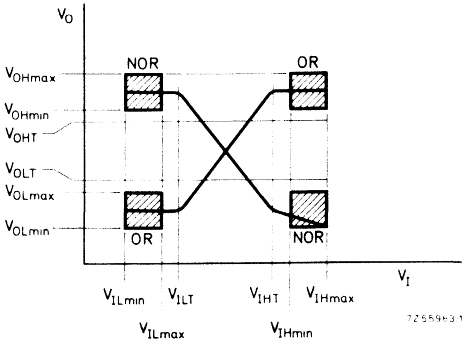
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5,2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are defined in the figure.

V_D = direct input voltage
V_I = invert input voltage

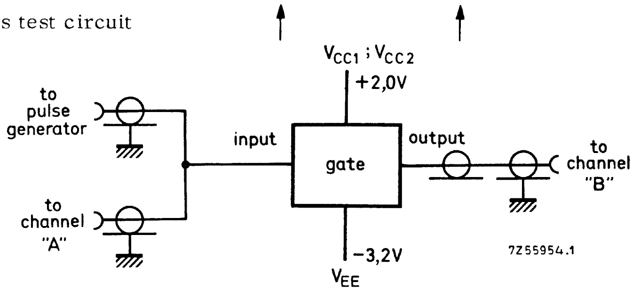


	Symbol		Tamb (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	−1000	−960	−900	mV	V_D = −2,09 V; V_I = −2,70 V
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1,870	−1,850	−1,830	V	V_D = −2,70 V; V_I = −2,09 V
		typ.	−	−1,720	−	V	
		max.	−1,665	−1,650	−1,625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	$V_D - V_I$ = 185 mV; V_D = −0,600 V to −3,065 V
Output threshold voltage LOW	V_{OLT}	max.	−1,645	−1,630	−1,605	V	$V_I - V_D$ = 185 mV; V_D = −0,785 V to −3,250 V
Input current HIGH	I_{IH}	typ.	−	40	−	μA	V_{IH} = −0,81 V
		max.	−	80	−	μA	
Supply current	I_{EE}	typ.	−	20	−	mA	V_D = −2,70 V; V_I = −2,09 V
		max.	−	25	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0,25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time	t_{pdr}	1,0	2,0	2,9	ns	pins 4, 7, 10, 13 connected to V_{BB}. See waveforms on page 5
Fall propagation delay time	t_{pdf}	1,0	2,0	2,9	ns	
Rise time	t_r	1,1	2,0	3,3	ns	See waveforms on page 5
Fall time	t_f	1,1	2,0	3,3	ns	
Input capacitance (see note 1)	C_I	–	–	5	pF	reflection measurement

Switching times test circuit

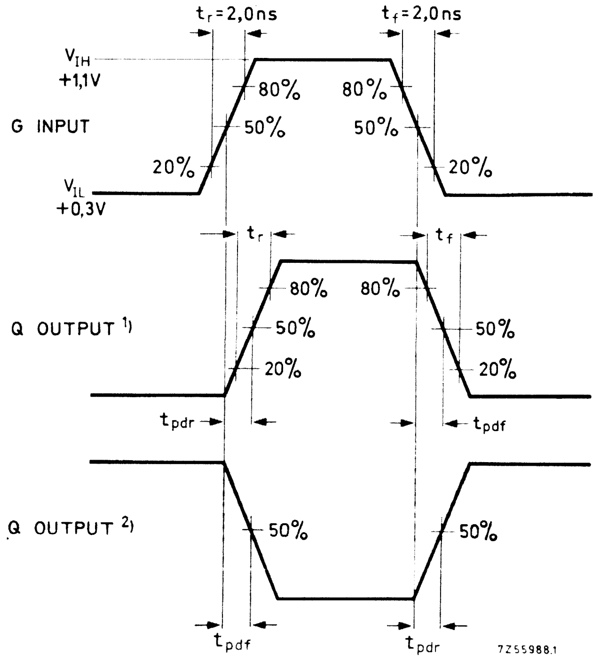


Notes

1. Input resistance is positive at any frequency.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal lengths.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

Switching times waveforms



1) Pulse generator connected to direct input. Invert inputs G_1, G_4, G_5 and G_8 connected to V_{BB}.

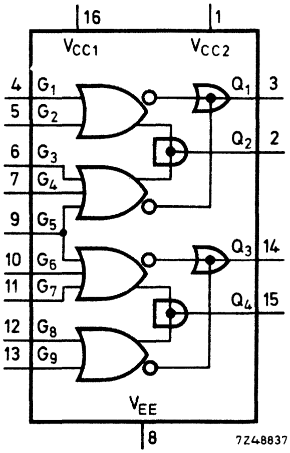
2) Pulse generator connected to invert input. Direct inputs G_2, G_3, G_6 and G_7 connected to V_{BB}.

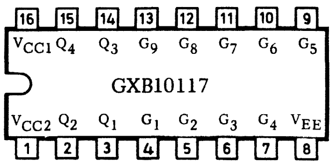
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10117 is a dual 2-wide 2-3 input OR-AND/OR-AND-INVERT gate designed for use in data control as a general purpose logic element.

The GX family corresponds to the ECL10 000series.

DUAL OR-AND/OR-AND-INVERT GATE





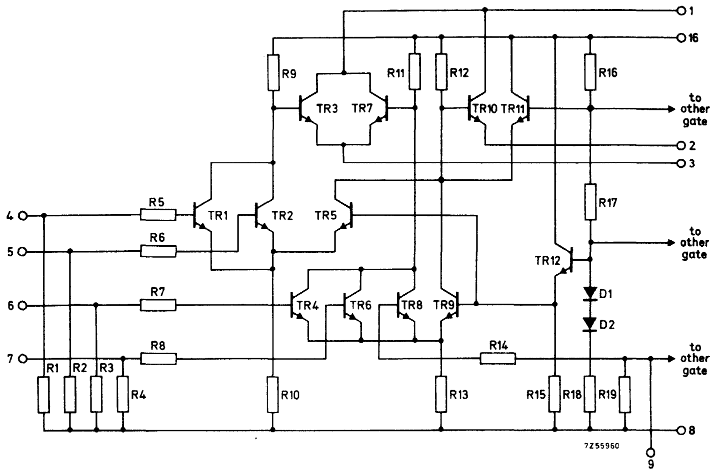
$V_{CC1} = V_{CC2} = 0$ V (ground)

$V_{EE} = -5,2$ V

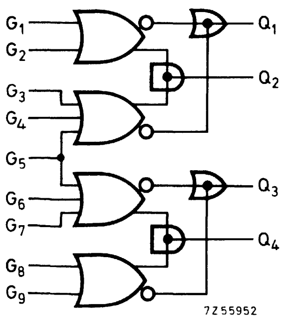
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		$-5,2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}		0 to +75	^{o}C
Average propagation delay	t_{pd}	typ.	2,3	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	100	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q_1 = \overline{(G_1+G_2) \cdot (G_3+G_4+G_5)}$

$Q_2 = (G_1+G_2) \cdot (G_3+G_4+G_5)$

$Q_3 = \overline{(G_8+G_9) \cdot (G_5+G_6+G_7)}$

$Q_4 = (G_8+G_9) \cdot (G_5+G_6+G_7)$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

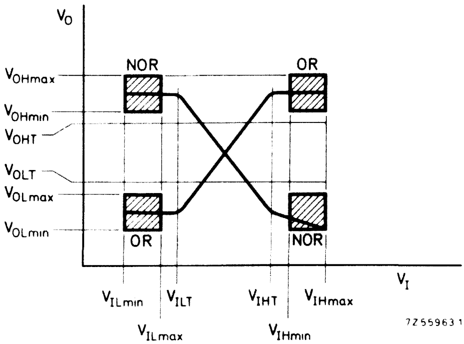
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	^oC
Junction temperature	T_j	max.	125	^oC

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2, 5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2, 0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	^oC
V_{IHmax}	−0, 840	−0, 810	−0, 720	V
V_{IHT}	−1, 145	−1, 105	−1, 045	V
V_{ILT}	−1, 490	−1, 475	−1, 450	V
V_{ILmin}	−1, 870	−1, 850	−1, 830	V

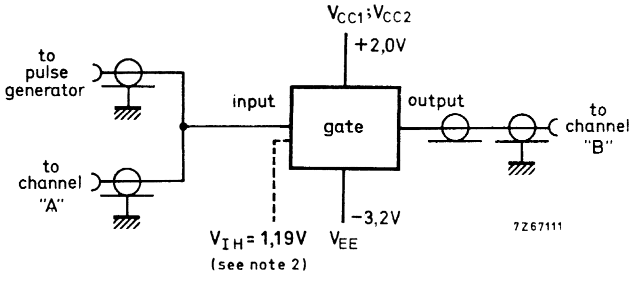


	Symbol		T_{amb} (^oC) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min	−1000	−960	−900	mV	V_{IHmax} or V_{ILmin}
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−2, 000	−1, 990	−1, 970	V	V_{ILmin} or V_{IHmax}
		typ.	−	−1, 720	−	V	
		max.	−1, 665	−1, 650	−1, 625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	V_{IHT} or V_{ILT}
Output threshold voltage LOW	V_{OLT}	max.	−1, 645	−1, 630	−1, 605	V	V_{ILT} or V_{IHT}
Input current HIGH	I_{IH}	pin 9 max.	−	355	−	μA	V_{IHmax} for input under test
		other inputs max.	−	265	−	μA	
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	20	−	mA	V_{ILmin} for all inputs
		max.	−	26	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0, 25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time; OR output	t_{pdrOR}	1,4	2,3	3,4	ns	See waveforms on page 5
Fall propagation delay time; OR output	t_{pdfOR}	1,4	2,3	3,4	ns	See waveforms on page 5
Rise propagation delay time; NOR output	t_{pdrNOR}	1,4	2,3	3,4	ns	See waveforms on page 5
Fall propagation delay time; NOR output	t_{pdfNOR}	1,4	2,3	3,4	ns	See waveforms on page 5
Rise time	t_r	1,1	2,2	4,0	ns	See waveforms on page 5
Fall time	t_f	1,1	2,2	4,0	ns	See waveforms on page 5
Input capacitance (see note 1)	C_I:					
	pin 9	–	–	7	pF	reflection measurement
	other pins	–	–	5	pF	reflection measurement

Switching times test circuit

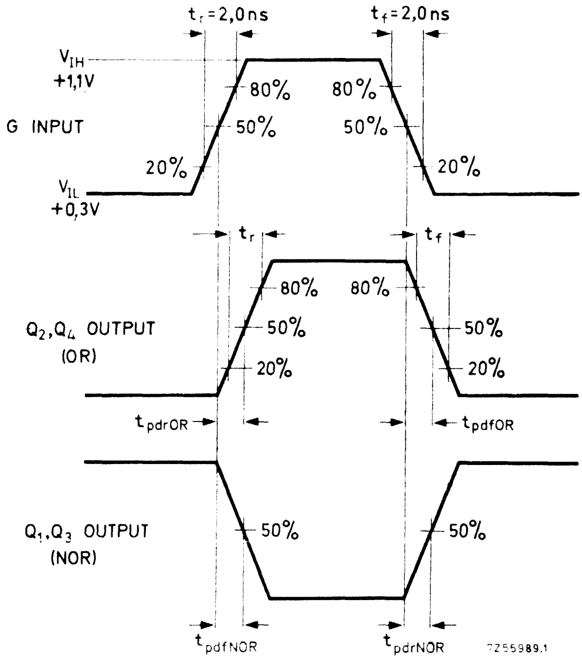


Notes

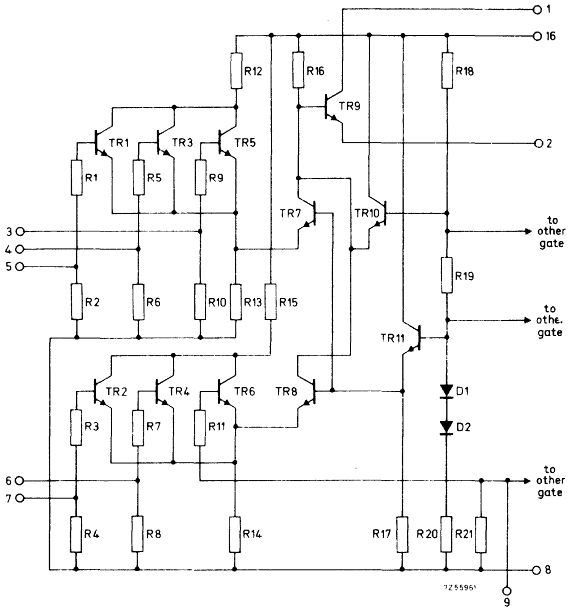
1. Input resistance is positive at any frequency.
2. In order to enable the output, at least one input of the other gates dotted to the gate under test must be HIGH.
3. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
4. Input impedance of the oscilloscope is 50 Ω.
5. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

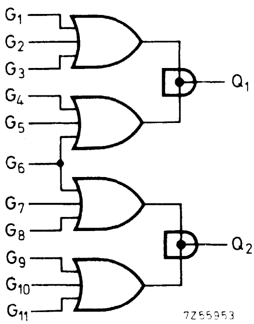
Switching times waveforms



CIRCUIT DIAGRAM (one gate)



LOGIC FUNCTION



$$Q_1 = (G_1 + G_2 + G_3) \cdot (G_4 + G_5 + G_6)$$

$$Q_2 = (G_6 + G_7 + G_8) \cdot (G_9 + G_{10} + G_{11})$$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

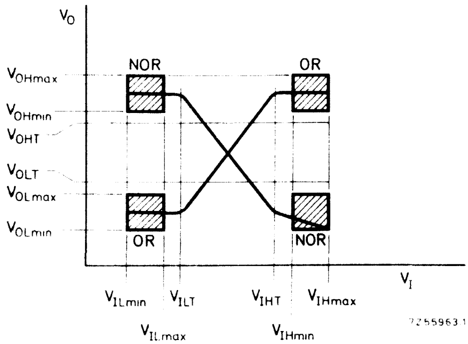
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2, 5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2, 0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0, 840	−0, 810	−0, 720	V
V_{IHT}	−1, 145	−1, 105	−1, 045	V
V_{ILT}	−1, 490	−1, 475	−1, 450	V
V_{ILmin}	−1, 870	−1, 850	−1, 830	V

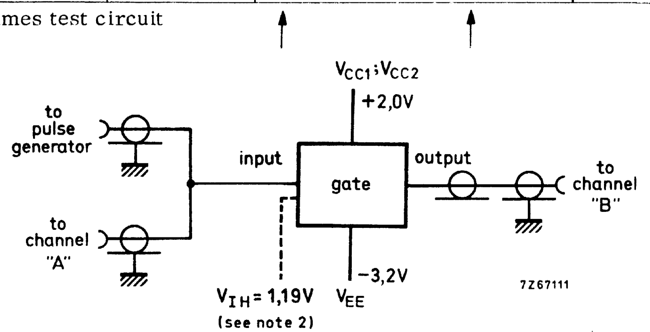


	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min	−1000	−960	−900	mV	Inputs at V_{IHmax}
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−2, 000	−1, 990	−1, 970	V	Inputs at V_{ILmin}
		typ.	−	−1, 720	−	V	
		max.	−1, 665	−1, 650	−1, 625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	Inputs at V_{IHT}
Output threshold voltage LOW	V_{OLT}	max.	−1, 645	−1, 630	−1, 605	V	Inputs at V_{ILT}
Input current HIGH	I_{IH} pin 9	max.	−	355	−	μA	V_{IHmax} for input under test
	I_{IH} other inputs	max.	−	265	−	μA	
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	20	−	mA	V_{ILmin} for all inputs
		max.	−	26	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0, 25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time	t_{pdr}	1,4	2,3	3,4	ns	See waveforms on page 5
Fall propagation delay time	t_{pdf}	1,4	2,3	3,4	ns	See waveforms on page 5
Rise time	t_r	1,5	2,5	4,0	ns	See waveforms on page 5
Fall time	t_f	1,5	2,5	4,0	ns	See waveforms on page 5
Input capacitance (see note 1)	C_I:					
	pin 9	–	–	7	pF	reflection measurement
	other inputs	–	–	5	pF	reflection measurement

Switching times test circuit

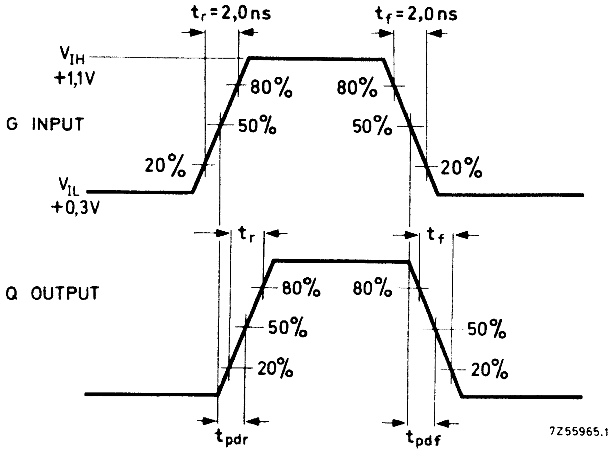


Notes

1. Input resistance is positive at any frequency.
2. In order to enable the output, at least one input of the other gates dotted to the gate under test must be HIGH.
3. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
4. Input impedance of the oscilloscope is 50 Ω.
5. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

Switching times waveforms

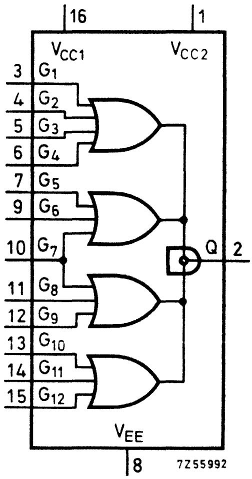


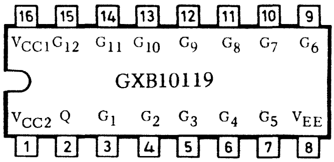
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10119 is a 4-wide 4-3-3-3-input OR-AND gate designed for use in data control as a general purpose logic element.

The GX family corresponds to the ECL 10 000 series.

OR-AND GATE





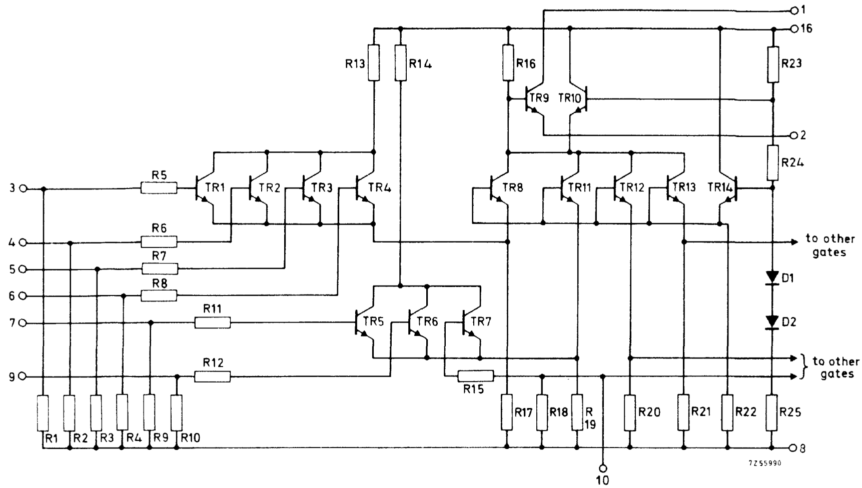
$V_{CC1} = V_{CC2} = 0$ V (ground)

$V_{EE} = -5,2$ V

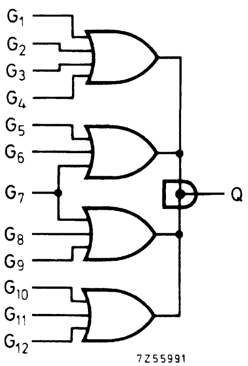
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		$-5,2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}		0 to +75	^{o}C
Average propagation delay	t_{pd}	typ.	2,3	ns
Output voltage HIGH state	V_{OH}	nom.	− 880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	100	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = (G_1 + G_2 + G_3 + G_4) \cdot (G_5 + G_6 + G_7) \cdot (G_7 + G_8 + G_9) \cdot (G_{10} + G_{11} + G_{12})$$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

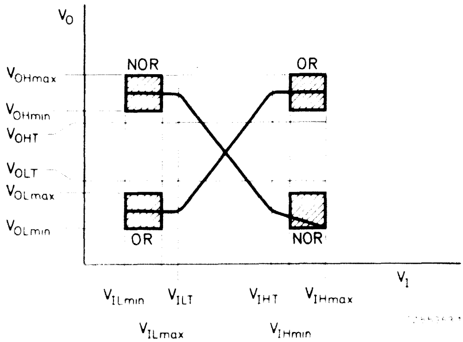
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5,2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0,840	−0,810	−0,720	V
V_{IHT}	−1,145	−1,105	−1,045	V
V_{ILT}	−1,490	−1,475	−1,450	V
V_{ILmin}	−1,870	−1,850	−1,830	V

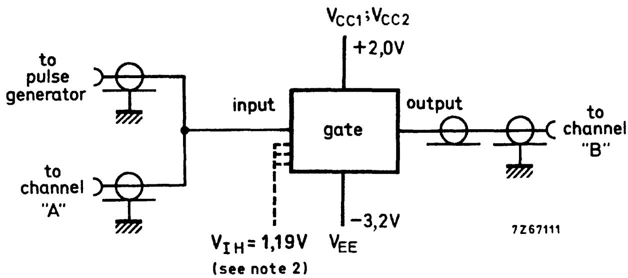


	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	−1000	−960	−900	mV	Inputs at V_{IHmax}
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−2,000	−1,990	−1,970	V	Inputs at V_{ILmin}
		typ.	−	−1,720	−	V	
		max.	−1,665	−1,650	−1,625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	Inputs at V_{IHT}
Output threshold voltage LOW	V_{OLT}	max.	−1,645	−1,630	−1,605	V	Inputs at V_{ILT}
Input current HIGH	I_{IH} pin 10	max.	−	355	−	μA	V_{IHmax} for input under test
	I_{IH} other inputs	max.	−	265	−	μA	
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	20	−	mA	V_{ILmin} for all inputs
		max.	−	26	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0,25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time	t_{pdr}	1,4	2,3	3,4	ns	See waveforms on page 5
Fall propagation delay time	t_{pdf}	1,4	2,3	3,4	ns	
Rise time	t_r	1,5	2,5	4,0	ns	
Fall time	t_f	1,5	2,5	4,0	ns	
Input capacitance (see note 1)	pin 10	–	–	7	pF	reflection measurement
	other pins	–	–	5	pF	

Switching times test circuit

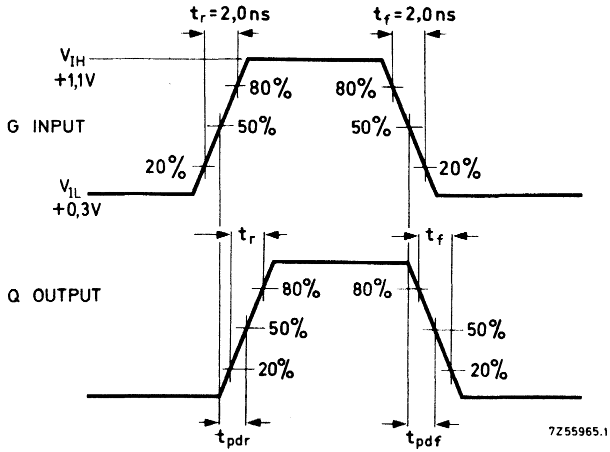


Notes

1. Input resistance is positive at any frequency.
2. In order to enable the output, at least one input of the other gates dotted to the gate under test must be HIGH.
3. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
4. Input impedance of the oscilloscope is 50 Ω.
5. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

Switching times waveforms

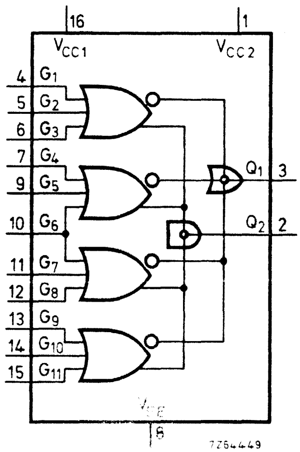


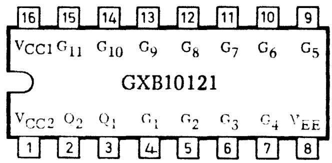
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10121 is a 4-wide OR-AND/OR-AND-INVERT gate designed for use in data control as a general purpose logic element.

Input pull-down resistors (50 kΩ) allow unused inputs to be left open.
The GX family corresponds to the ECL10 000series.

4-WIDE OR-AND/OR-AND-INVERT GATE





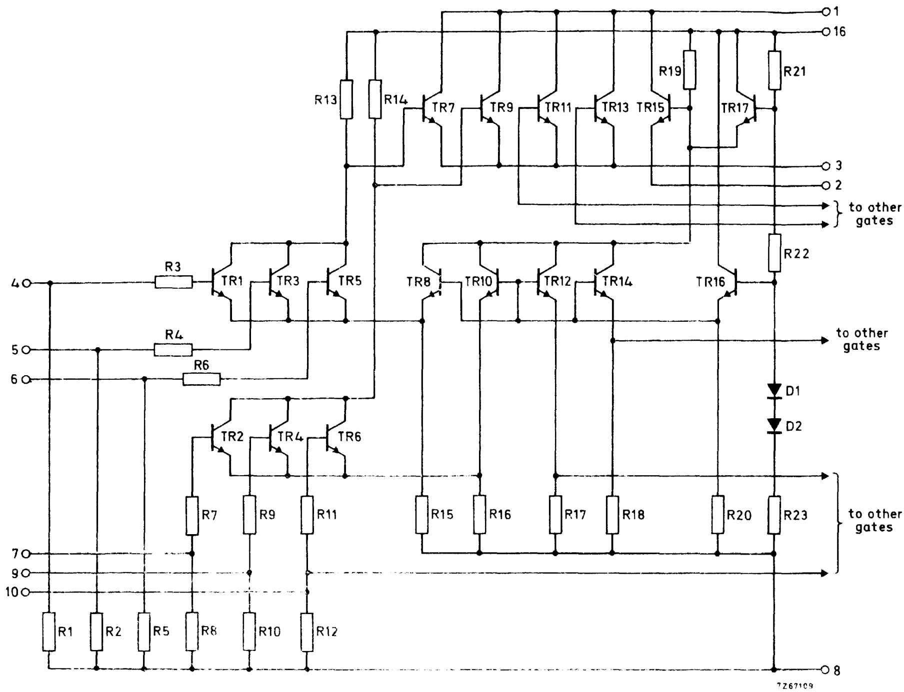
$V_{CC1} = V_{CC2} = 0$ V (ground)

$V_{EE} = -5,2$ V

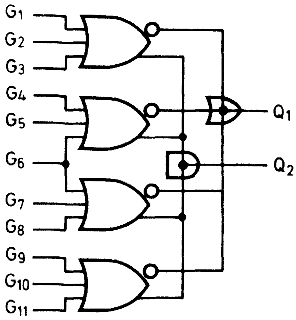
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		$-5,2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	2,3	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	100	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION



7Z67110

$$Q_1 = \overline{G_1 + G_2 + G_3} + \overline{G_4 + G_5 + G_6} + \overline{G_6 + G_7 + G_8} + \overline{G_9 + G_{10} + G_{11}}$$

$$Q_2 = \overline{Q}_1$$

positive logic: HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

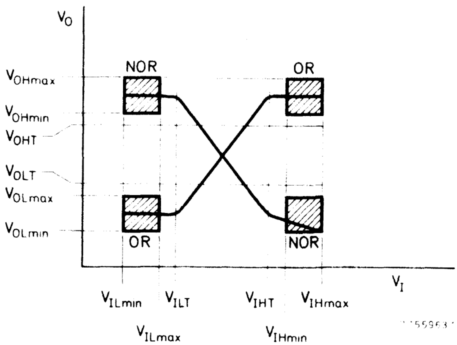
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5,2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0,840	−0,810	−0,720	V
V_{IHT}	−1,145	−1,105	−1,045	V
V_{ILT}	−1,490	−1,475	−1,450	V
V_{ILmin}	−1,870	−1,850	−1,830	V



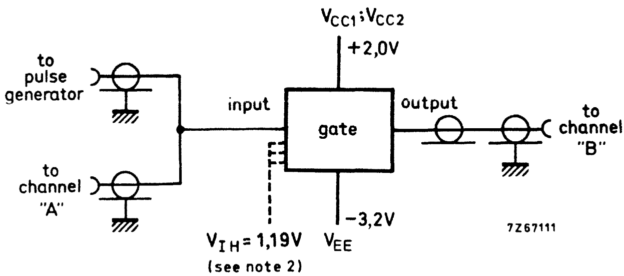
CHARACTERISTICS (continued)

	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	-1000	-960	-900	mV	V_{ILmin} on inputs for invert output V_{IHmax} on inputs for direct output
		typ.	–	-880	–	mV	
		max.	-840	-810	-720	mV	
Output voltage LOW	V_{OL}	min.	-2,000	-1,990	-1,970	V	V_{ILmin} on inputs for direct output V_{IHmax} on inputs for invert output
		typ.	–	-1,720	–	V	
		max.	-1,665	-1,650	-1,625	V	
Output threshold voltage HIGH	V_{OHT}	min.	-1020	-980	-920	mV	V_{ILT} on inputs for invert output V_{IHT} on inputs for direct output
Output threshold voltage LOW	V_{OLT}	max.	-1,645	-1,630	-1,605	V	V_{ILT} on inputs for direct output V_{IHT} on inputs for invert output
Input current HIGH	I_{IH}	pin 10 max.	–	355	–	μA	V_{IHmax} for input under test
		other inputs max.	–	265	–	μA	
Input current LOW	I_{IL}	min.	–	10	–	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	–	20	–	mA	V_{ILmin} for all inputs
		max.	–	26	–	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	–	0,25	–		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol		min.	typ.	max.		Conditions
Rise propagation delay times:							
OR output	t_{pdrOR}		1,4	2,3	3,4	ns	See waveforms on page 6
NOR output	t_{pdrNOR}		1,4	2,3	3,4	ns	See waveforms on page 6
Fall propagation delay times:							
OR output	t_{pdfOR}		1,4	2,3	3,4	ns	See waveforms on page 6
NOR output	t_{pdfNOR}		1,4	2,3	3,4	ns	See waveforms on page 6
Rise time	t_r		1,1	2,5	4,0	ns	See waveforms on page 6
Fall time	t_f		1,1	2,5	4,0	ns	See waveforms on page 6
Input capacitance (see note 1)	C_I	pin 10	–	–	7	pF	reflection measurement
		other inputs	–	–	5	pF	reflection measurement

Switching times test circuit

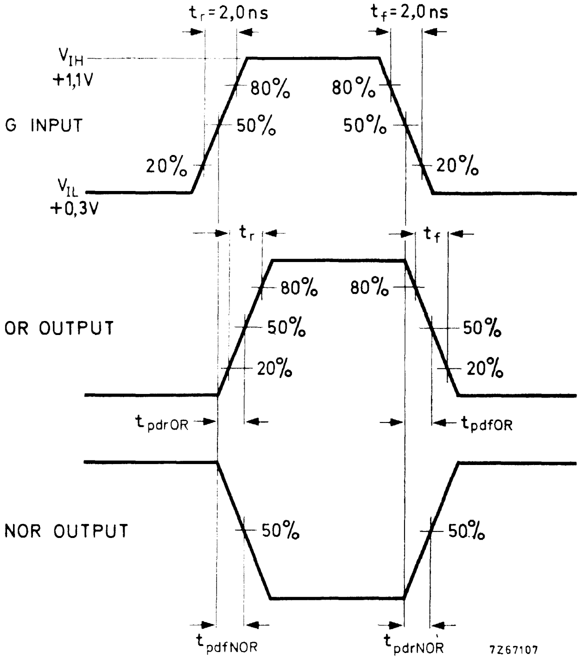


Notes

1. Input resistance is positive at any frequency.
2. In order to enable the output, at least one input of the other gates dotted to gate under test shall be HIGH.
3. Input and output cables the oscilloscope are 50 Ω coaxial cables with equal length.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.
5. Input impedance of the oscilloscope is 50 Ω.

CHARACTERISTICS (continued)

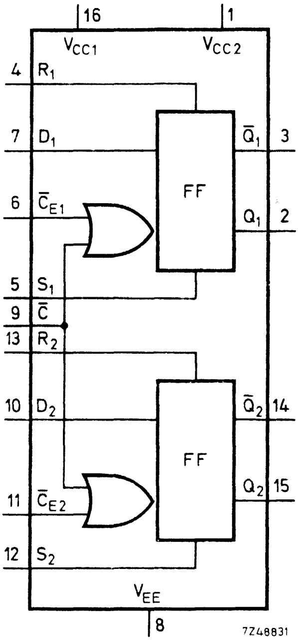
Switching times waveforms



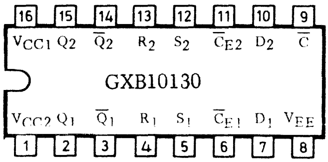
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10130 is a clocked dual D-type latch. Each element can be clocked separately by holding the common clock in the LOW state and using the clock enable inputs for the clocking function. The outputs are latched when the level of the clock is high.

The GX family corresponds to the ECL10 000series.



DUAL D-LATCH

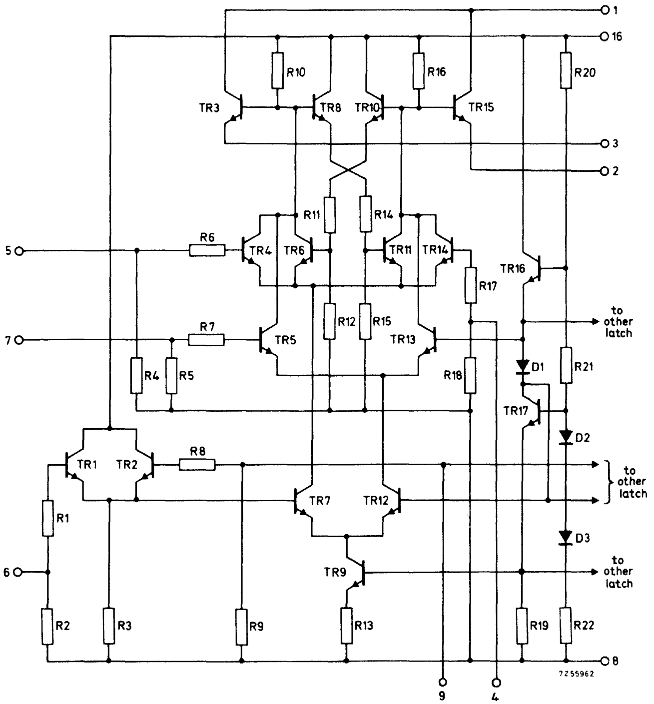


$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5,2$ V

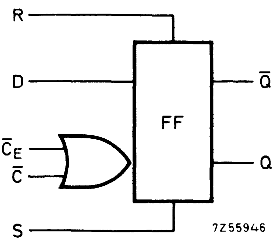
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		$-5,2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}		0 to +75	^{o}C
Average propagation delay	t_{pd}	typ.	2,0	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	110	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM (one latch)



FUNCTION TABLES



Synchronous operation

D_n	$\overline{C}$	$\overline{C_E}$	Q_{n+1} *)
L	L	L	L
L	L	H	Q_n
L	H	L	Q_n
L	H	H	Q_n
H	L	L	H
H	L	H	Q_n
H	H	L	Q_n
H	H	H	Q_n

*) R + S = LOW

Asynchronous operation
($\overline{C}$ or $\overline{C}_E$ = HIGH)

R	S	Q_1
L	L	Q
L	H	H
H	L	L
H	H	**)

**) not allowed

HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

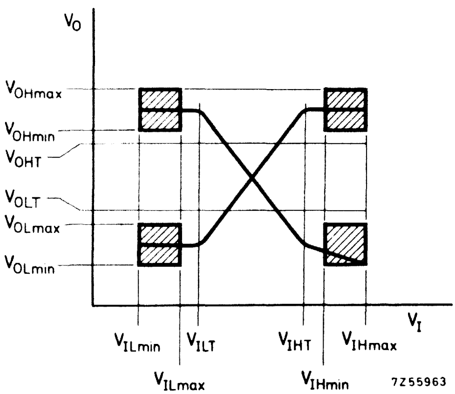
Supply voltage (d.c.)	V_{EE}	max.	−8, 0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	^oC
Junction temperature	T_j	max.	125	^oC

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2, 5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2, 0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	^oC
V_{IHmax}	−0, 840	−0, 810	−0, 720	V
V_{IHT}	−1, 145	−1, 105	−1, 045	V
V_{ILT}	−1, 490	−1, 475	−1, 450	V
V_{ILmin}	−1, 870	−1, 850	−1, 830	V



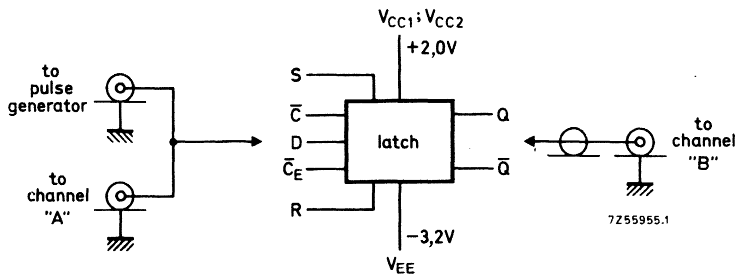
CHARACTERISTICS (continued) (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	−1000	−960	−900	mV	S at V_{IHmax}, R at V_{ILmin} or D at V_{IHmax}, $\overline{C}$, $\overline{C}_E$ at V_{ILmin}
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1, 870	−1, 850	−1, 830	V	R at V_{IHmax}, S at V_{ILmin} or D at V_{ILmin}, $\overline{C}$, $\overline{C}_E$ at V_{ILmin}
		typ.	−	−1, 720	−	V	
		max.	−1, 665	−1, 650	−1, 625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	S at V_{IHT} or D at V_{IHT}, $\overline{C}$, $\overline{C}_E$ at V_{ILT}
Output threshold voltage LOW	V_{OLT}	max.	−1, 645	−1, 630	−1, 605	V	R at V_{IHT} or D at V_{ILT}, $\overline{C}$, $\overline{C}_E$ at V_{ILT}
Input current HIGH	I_{IH} pin 9	max.	−	355	−	μA	V_{IHmax} for input under test
	I_{IH} other inputs	max.	−	265	−	μA	
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	22	−	mA	V_{ILmin} for all inputs
		max.	−	30	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0, 25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5, 2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time						
S Q	t_{pdr}	1,0	2,0	3,5	ns	See waveforms on page 6
R Q	t_{pdr}	1,0	2,0	3,5	ns	
$\overline{C}$ Q	t_{pdr}	1,5	3,0	4,5	ns	
$\overline{C}$ $\overline{Q}$	t_{pdr}	1,5	3,0	4,5	ns	
D Q	t_{pdr}	1,0	2,0	3,5	ns	
D $\overline{Q}$	t_{pdr}	1,0	2,0	3,5	ns	
Fall propagation delay time						
S $\overline{Q}$	t_{pdf}	1,0	2,0	3,5	ns	
R Q	t_{pdf}	1,0	2,0	3,5	ns	
$\overline{C}$ Q	t_{pdf}	1,5	3,0	4,5	ns	
$\overline{C}$ $\overline{Q}$	t_{pdf}	1,5	3,0	4,5	ns	
D Q	t_{pdf}	1,0	2,0	3,5	ns	
D $\overline{Q}$	t_{pdf}	1,0	2,0	3,5	ns	
Rise time	t_r	1,1	2,1	3,5	ns	
Fall time	t_f	1,1	2,1	3,5	ns	
Input capacitance (see note 1)	C_I:					reflection measurement
	pin 9	−	−	7	pF	
	other inputs	−	−	5	pF	

Switching times test circuit

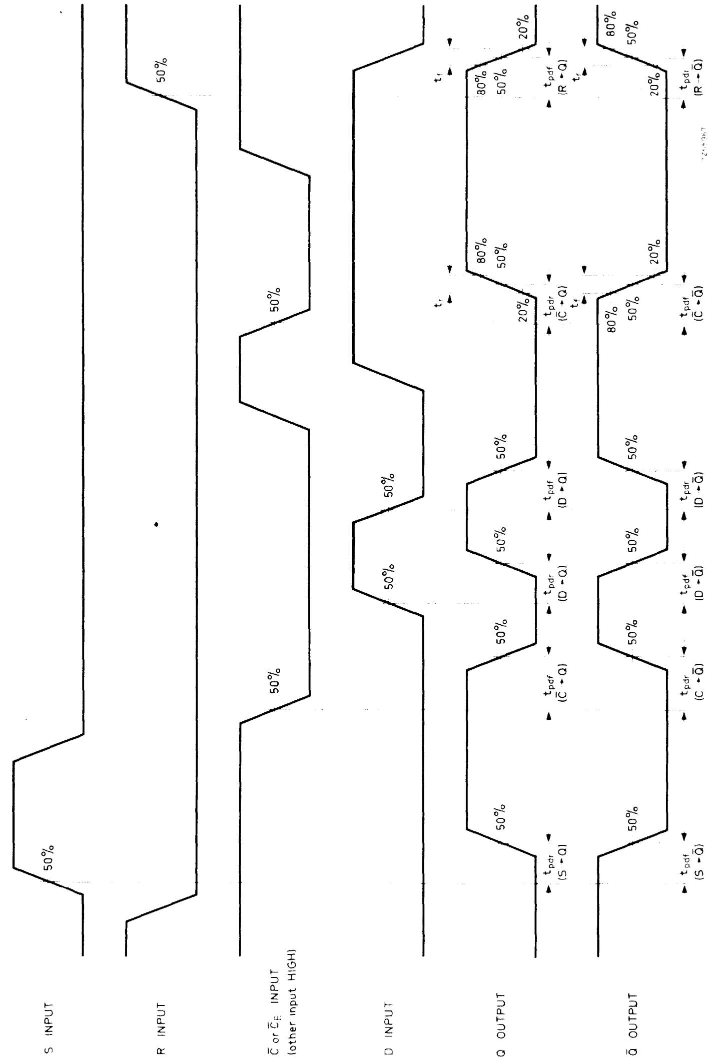


Notes

1. Input resistance is positive at any frequency.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

CHARACTERISTICS (continued)

Switching times waveforms



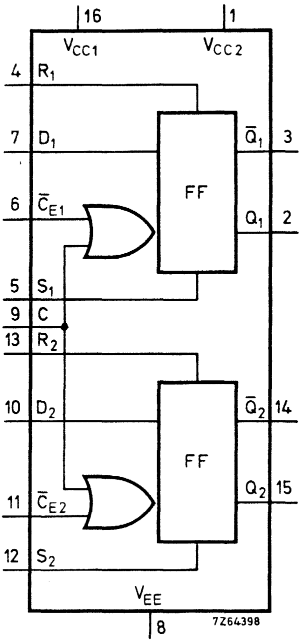
Conditions for input signals: $t_r = t_f = 2,0$ ns (20% to 80%); $V_{IH} = +1,1$ V; $V_{IL} = +0,3$ V

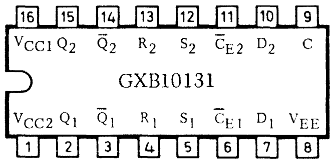
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is reconnnended for high speed large system design.

The GXB10131 is a dual master-slave D-type flip-flop. Each flip-flop can be clocked separately by holding the common clock in the LOW state and using the clock enable inputs for the clocking function. The output states of the flip-flops change when the level of the clock is high.

The GX family corresponds to the ECL 10 000 series.

DUAL D-TYPE MASTER-SLAVE FLIP-FLOP



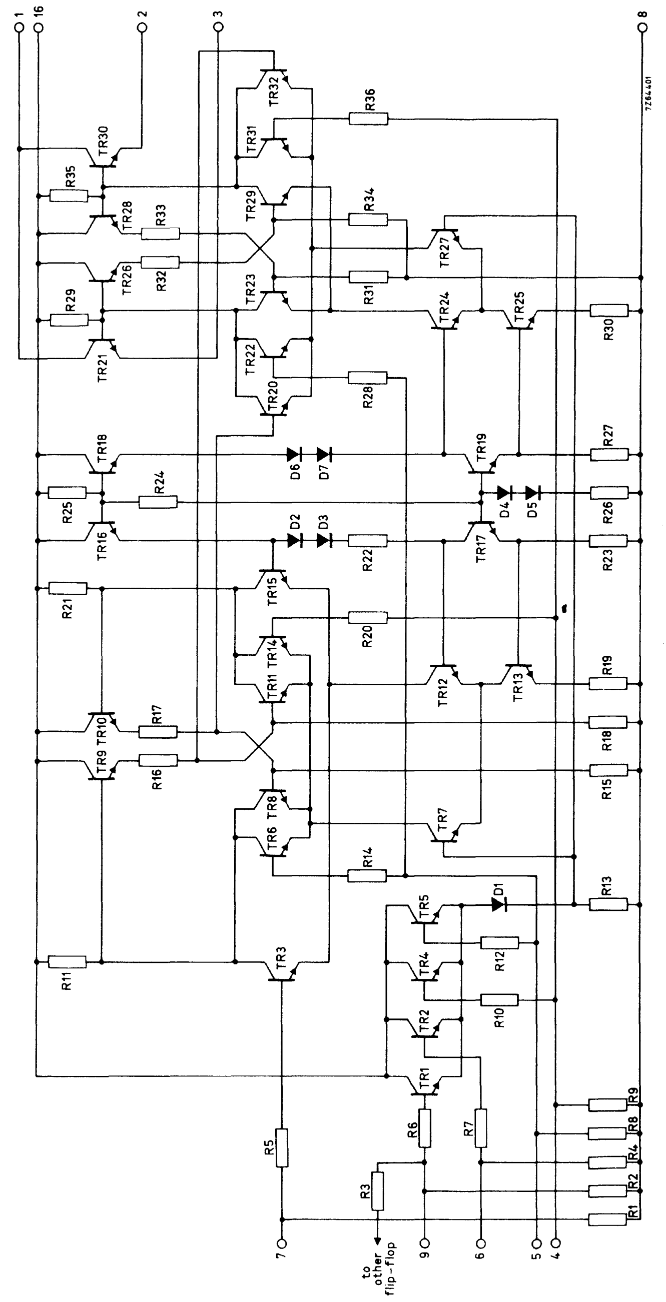


$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5,2$ V

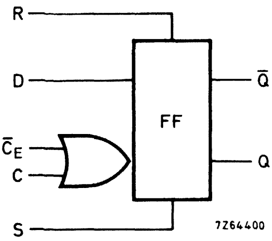
QUICK REFERENCE DATA				
Supply voltage	V_{EE}		−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Clock frequency	f	typ.	160	MHz
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	230	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLES



Synchronous operation 1)

D_n	C	$\overline{C}_E$	Q_{n+1} 2)
L	L	L	Q_n
L	L	H	Q_n
L	H	L	L
L	H	H	Q_n
H	L	L	Q_n
H	L	H	Q_n
H	H	L	H
H	H	H	Q_n

Asynchronous operation

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	3)

Positive logic:

HIGH state = 1
LOW state = 0

Notes

1. Conditions for C and $\overline{C}_E$ may be interchanged. In this table $\overline{C}_E$ is static, while for C a H represents a transition from L to H between t_n and t_{n+1}.
2. R + S = LOW
3. Not allowed.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

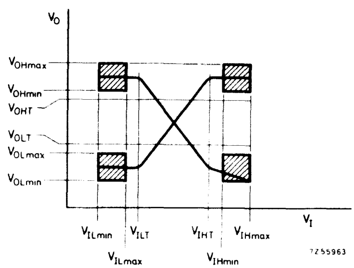
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5,2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0,840	−0,810	−0,720	V
V_{IHT}	−1,145	−1,105	−1,045	V
V_{ILT}	−1,490	−1,475	−1,450	V
V_{ILmin}	−1,870	−1,850	−1,830	V



CHARACTERISTICS (continued) (d.c.) at V_{CC} = ground; V_{EE} = −5,2 V

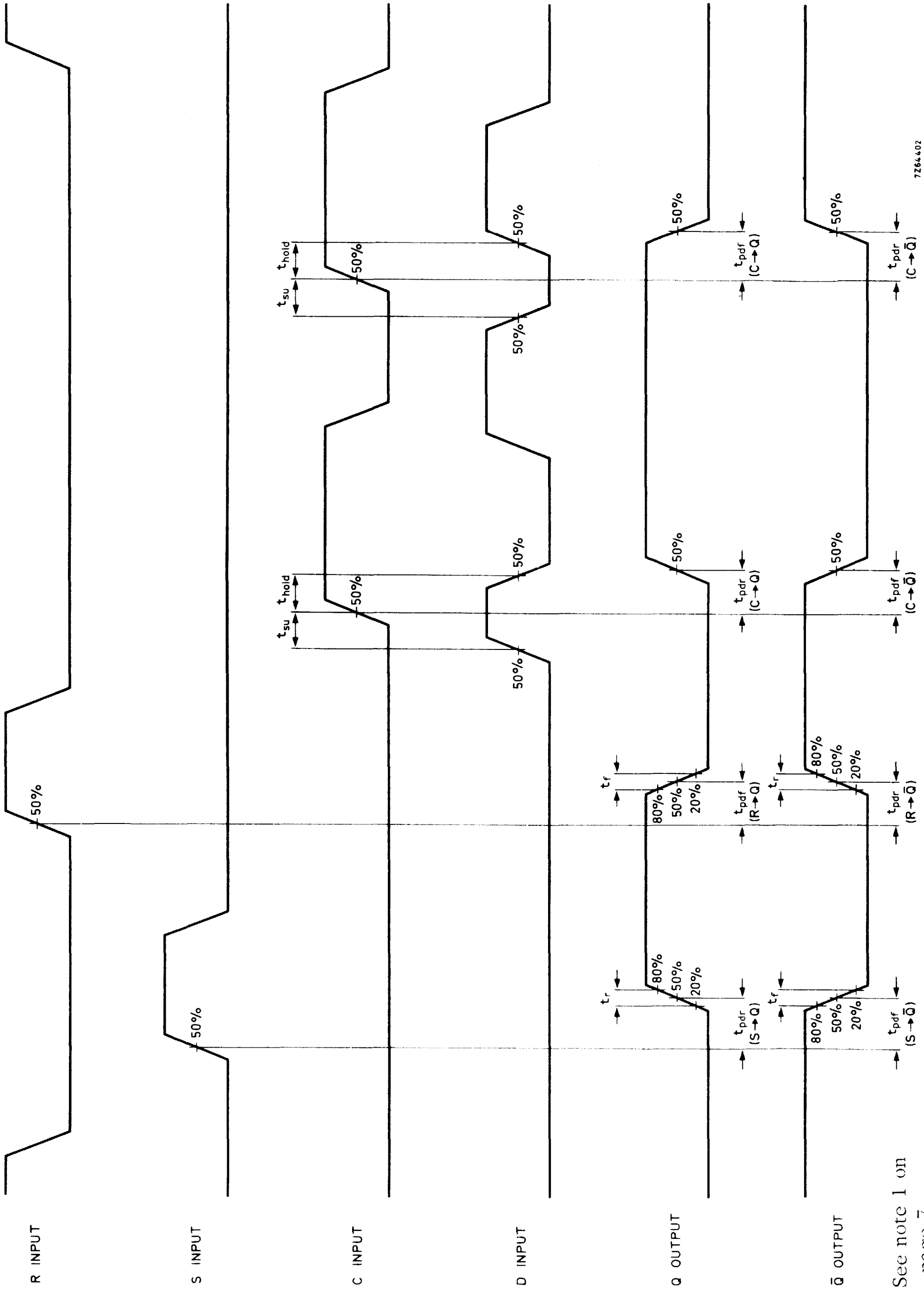
	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	−1000	−960	−900	mV	S at V_{IHmax} R at V_{ILmin} or $\bar{D}$ at V_{IHmax} $\bar{C}_E$ at V_{ILmin} C at $V_{IL} \rightarrow V_{IH}$
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1,870	−1,850	−1,830	V	S at V_{ILmin} R at V_{IHmax} or $\bar{D}$ at V_{ILmin} $\bar{C}_E$ at V_{ILmin} C at $V_{IL} \rightarrow V_{IH}$
		typ.	−	−1,720	−	V	
		max.	−1,665	−1,650	−1,625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	S at V_{IHT} R at V_{ILT} or $\bar{D}$ at V_{IHT} $\bar{C}_E$ at V_{ILT} C at $V_{ILT} \rightarrow V_{IHT}$
Output threshold voltage LOW	V_{OLT}	max.	−1,645	−1,630	−1,605	V	S at V_{ILT} R at V_{IHT} or $\bar{D}$ at V_{ILT} $\bar{C}_E$ at V_{ILT} C at $V_{ILT} \rightarrow V_{IHT}$
Input current HIGH	I_{IH} pin 9	max.	−	355	−	μA	V_{IHmax} for input under test
	I_{IH} other inputs	max.	−	265	−	μA	
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	45	−	mA	V_{ILmin} for all inputs
		max.	−	56	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0,25	−		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5, 2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time						
S → Q	t_{pdr}	1,2	2,8	4,3	ns	See waveforms on page 6
R → $\overline{Q}$	t_{pdr}	1,2	2,8	4,3	ns	
C → Q	t_{pdr}	1,5	3,0	4,5	ns	
C → $\overline{Q}$	t_{pdr}	1,5	3,0	4,5	ns	
Fall propagation delay time						
S → $\overline{Q}$	t_{pdf}	1,2	2,8	4,3	ns	
R → Q	t_{pdf}	1,2	2,8	4,3	ns	
C → Q	t_{pdf}	1,5	3,0	4,5	ns	
C → $\overline{Q}$	t_{pdf}	1,5	3,0	4,5	ns	
Rise time	t_r	1,1	2,0	4,5	ns	
Fall time	t_f	1,1	2,0	4,5	ns	
Set-up time	t_{su}	-	1,5	2,5	ns	
Hold time	t_{hold}	-	−0,5	1,5	ns	
Clock frequency	f	125	160	-	MHz	
Input capacitance (see note)	C_I (pin 7;10)	-	-	7	pF	reflection measurement
	C_I (pin 9;4; 5;12;13)	-	-	8	pF	

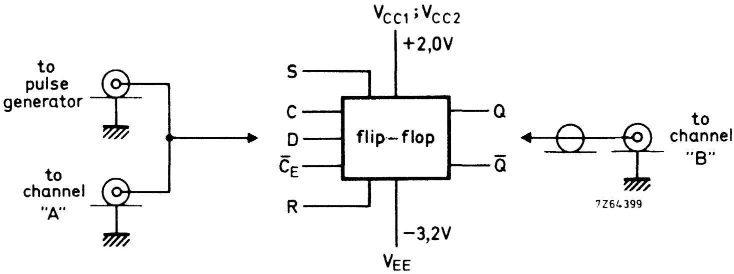
↑ (min.) ↑ (max.)

Note: Input resistance is positive at any frequency

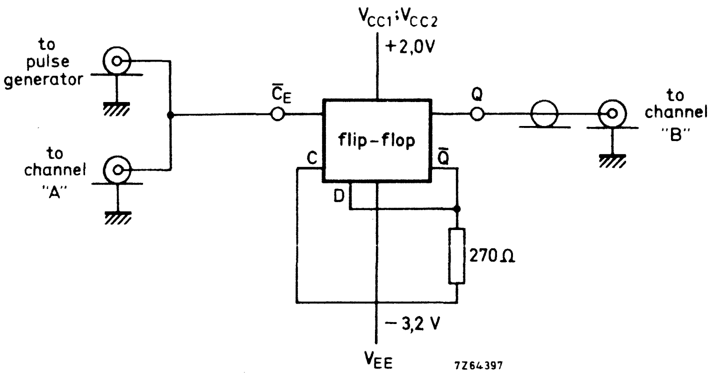


See note 1 on page 7.

Switching times test circuits



Measurement of propagation delay



Measurement of clock frequency

Notes

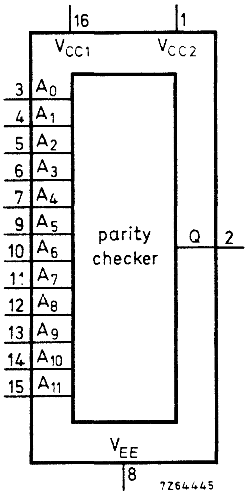
1. Input signal: $t_r = t_f = 2,0$ ns (20% to 80%); $V_{IH} = +1,1$ V; $V_{IL} = +0,3$ V.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

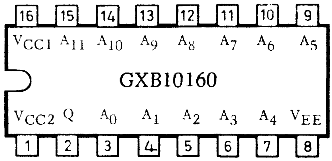
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10160 is a 12-bit parity checker or generator. The output goes HIGH when an odd number of inputs are HIGH.
If parity detection or generation is required for less than 12 bits, the unused inputs can be left open (50 kΩ input pull-down resistors).

The GX family corresponds to the ECL10000series.

12-BIT PARITY CHECKER/GENERATOR



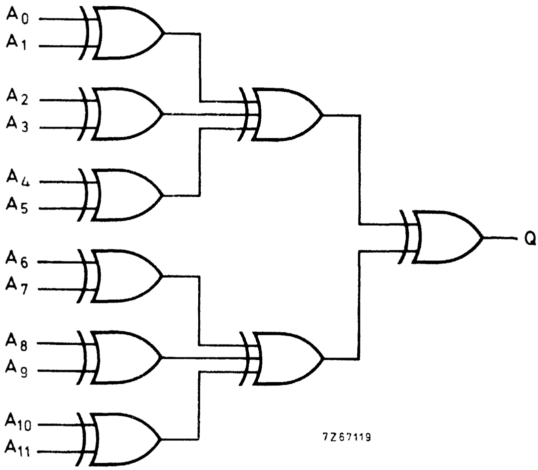


$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5,2$ V

QUICK REFERENCE DATA				
Supply voltage	V_{EE}		−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	4,5	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	310	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

LOGIC DIAGRAM



LOGIC FUNCTION

$$Q = A_0 \oplus A_1 \oplus A_2 \oplus A_3 \oplus A_4 \oplus A_5 \oplus A_6 \oplus A_7 \oplus A_8 \oplus A_9 \oplus A_{10} \oplus A_{11}$$

FUNCTION TABLE

summ of inputs at HIGH state	Q
odd	H
even	L

positive logic:

HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

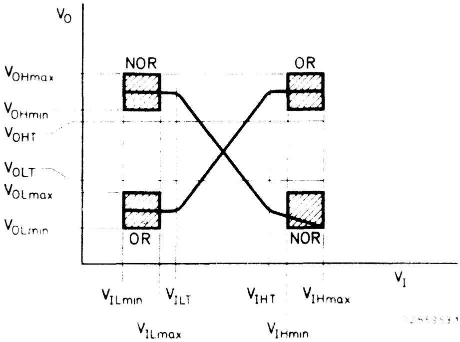
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0, 840	−0, 810	−0, 720	V
V_{IHT}	−1, 145	−1, 105	−1, 045	V
V_{ILT}	−1, 490	−1, 475	−1, 450	V
V_{ILmin}	−1, 870	−1, 850	−1, 830	V

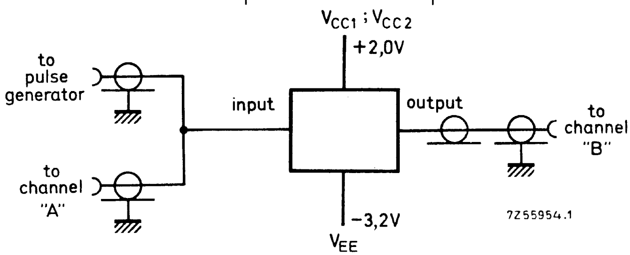


	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	−1000	−960	−900	mV	odd number of inputs at V_{IHmax}; other inputs at V_{ILmin}
		typ.	–	−880	–	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1, 870	−1, 850	−1, 830	V	even number of inputs at V_{IHmax}; other inputs at V_{ILmin}
		typ.	–	−1, 720	–	V	
		max.	−1, 665	−1, 650	−1, 625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	one input at V_{IHT}; other inputs at V_{ILmin}
Output threshold voltage LOW	V_{OLT}	max.	−1, 645	−1, 630	−1, 605	V	one input at V_{ILT}; other inputs at V_{ILmin}
Input current HIGH	I_{IH}	max.	–	265	–	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}	min.	–	10	–	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	–	62	–	mA	all inputs at V_{ILmin}
		max.	–	70	–	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	–	0, 25	–		

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time	t_{pdr}	2,0	4,5	7,5	ns	See waveforms on page 5
Fall propagation delay time	t_{pdf}	2,0	4,5	7,5	ns	
Rise time	t_r	1,1	2,0	3,3	ns	
Fall time	t_f	1,1	2,0	3,3	ns	
Input capacitance (see note 1)	C_I	–	–	5	pF	reflection measurement

Switching times test circuit

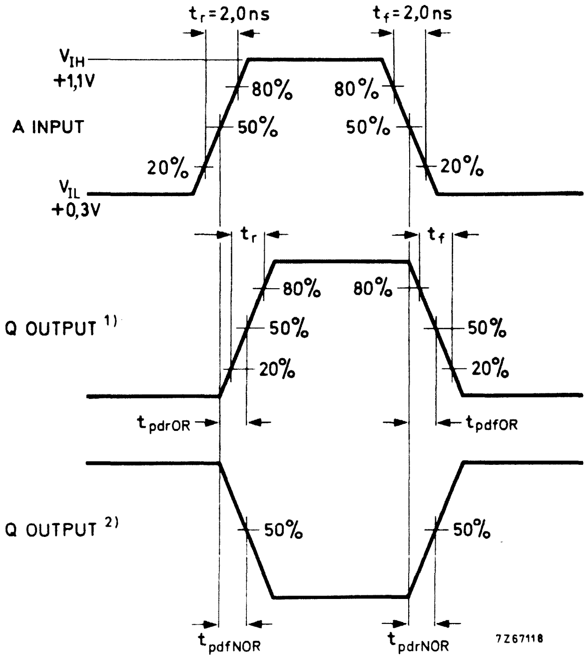


Notes

1. Input resistance is positive at any frequency.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.
4. Input impedance of the oscilloscope is 50 Ω.

CHARACTERISTICS (continued)

Switching times test waveforms



1) Even number of other inputs HIGH.

2) Odd number of other inputs HIGH.

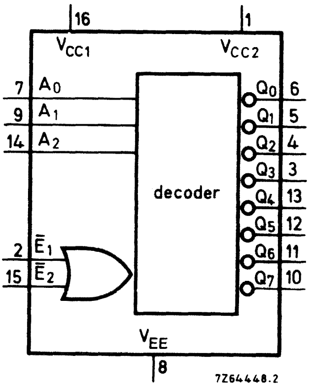
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

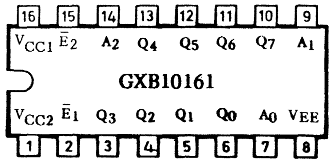
The GXB10161 is a three-bit decoder with two enable inputs.

The GX family corresponds to the ECL10 000series.

THREE-BIT DECODER

one of eight lines LOW





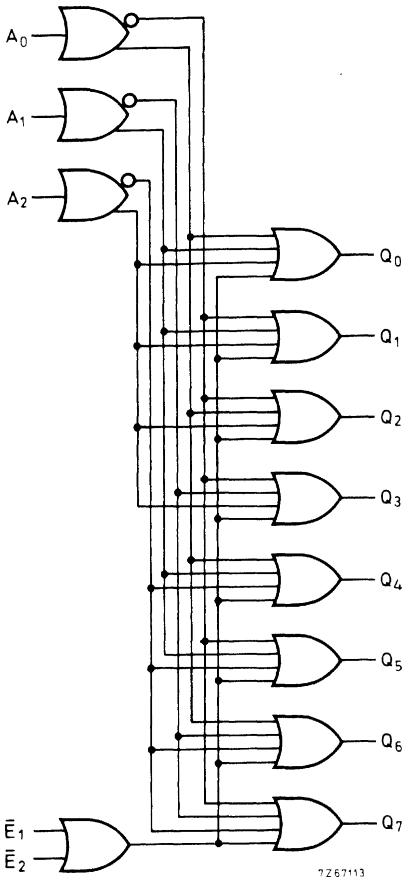
$V_{CC1} = V_{CC2} = 0$ V (ground)

$V_{EE} = -5,2$ V

QUICK REFERENCE DATA				
Supply voltage	V_{EE}		$-5,2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}		0 to +75	^{o}C
Average propagation delay	t_{pd}	typ.	4,0	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	490	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

LOGIC DIAGRAM



PIN NAMES

A_0 to A_2 : binary inputs
Q_0 to Q_7 : decoded outputs
$\overline{E}_1$; $\overline{E}_2$: enable inputs

FUNCTION TABLE

enable inputs		binary inputs			decimal outputs							
$\overline{E}_1$	$\overline{E}_2$	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
H	H	X	X	X	H	H	H	H	H	H	H	H
L	H	X	X	X	H	H	H	H	H	H	H	H
H	L	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L

positive logic:

HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

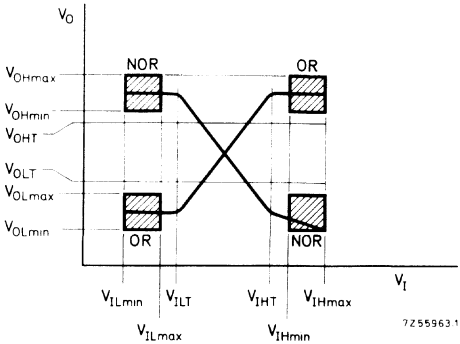
Supply voltage (d.c.)	V_{EE}	max.	−8.0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5,2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0,840	−0,810	−0,720	V
V_{IHT}	−1,145	−1,105	−1,045	V
V_{ILT}	−1,490	−1,475	−1,450	V
V_{ILmin}	−1,870	−1,850	−1,830	V



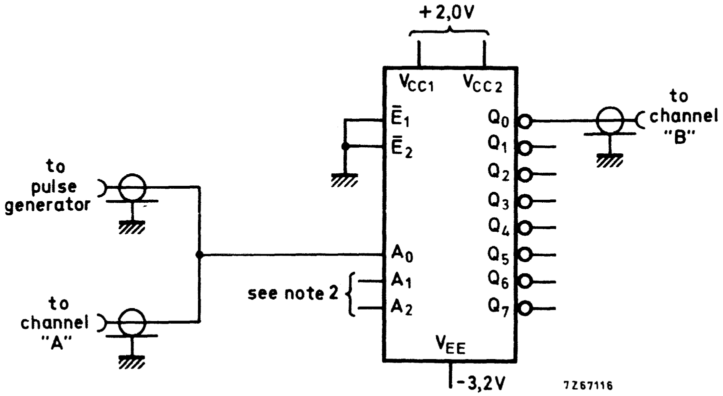
	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	−1000	−960	−900	mV	one $\bar{E}$ input at V_{IHmax}; other $\bar{E}$ input at V_{ILmin}
		typ.	–	−880	–	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1,870	−1,850	−1,830	V	all inputs at V_{ILmin} for Q_0
		typ.	–	−1,720	–	V	
		max.	−1,665	−1,650	−1,625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	one $\bar{E}$ input at V_{IHT}; other $\bar{E}$ inputs at V_{ILmin}
Output threshold voltage LOW	V_{OLT}	max.	−1,645	−1,630	−1,605	V	one A input at V_{IHT} or V_{ILT}; other A inp. at V_{ILmin} or V_{IHmax} [1])
Input current HIGH	I_{IH}	max.	–	265	–	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}	min.	–	10	–	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	–	95	–	mA	all inputs at V_{ILmin}
		max.	–	125	–	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	–	0,25	–		

[1]) See also function table on page 3.

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time	t_{pdr}	1,5	4,0	6,0	ns	See waveforms on page 6
Fall propagation delay time	t_{pdf}	1,5	4,0	6,0	ns	See waveforms on page 6
Rise time	t_r	1,1	2,0	3,3	ns	See waveforms on page 6
Fall time	t_f	1,1	2,0	3,3	ns	See waveforms on page 6
Input capacitance (see note 1)	C_I	–	–	5	pF	reflection measurement

Switching times test circuit

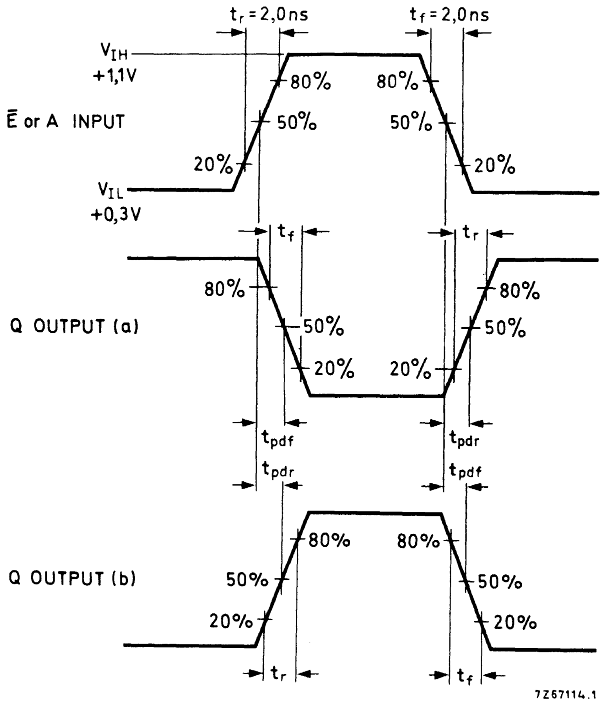


Notes

1. Input resistance is positive at any frequency.
2. Other A inputs are at +1,1 V or ground depending on output under test.
3. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.
5. Input impedance of the oscilloscope is 50 Ω.

CHARACTERISTICS (continued)

Switching times waveforms



Output waveform (a) or (b) depending on particular input and output under test.

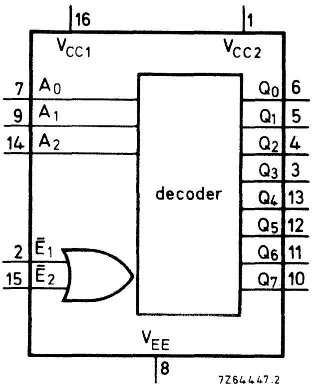
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

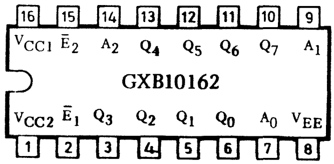
The GXB10162 is a three-bit decoder with two enable inputs.

The GX family corresponds to the ECL10 000series.

THREE-BIT DECODER

one of eight lines HIGH





V_{CC1} = V_{CC2} = 0 V (ground)

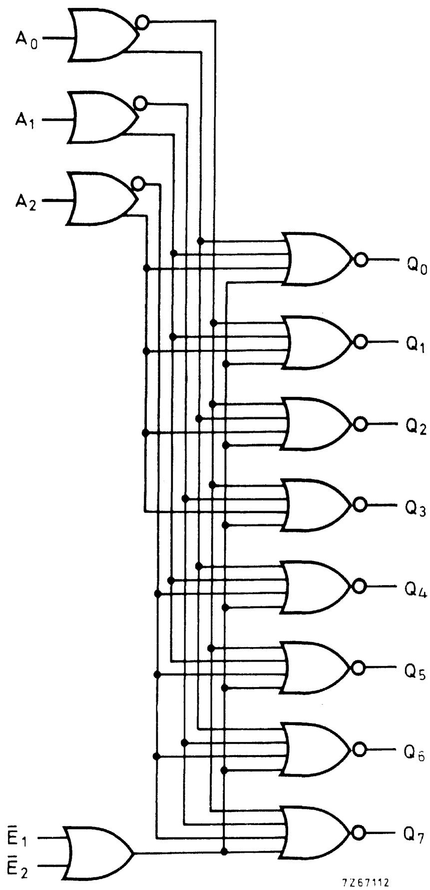
V_{EE} = −5, 2 V

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5, 2 ± 10%	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	4, 0	ns
Output voltage HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package	P_{av}	typ.	490	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

LOGIC DIAGRAM



PIN NAMES

A_0 to A_2 : binary inputs
Q_0 to Q_7 : decoded outputs
$\bar{E}_1$; $\bar{E}_2$: enable inputs

FUNCTION TABLE

enable inputs		binary inputs			decimal outputs							
$\overline{E}_1$	$\overline{E}_2$	A_0	A_1	A_3	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
H	H	X	X	X	L	L	L	L	L	L	L	L
L	H	X	X	X	L	L	L	L	L	L	L	L
H	L	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	L	L	L	L	H	L	L	L	L
L	L	L	L	H	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

positive logic: H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

HIGH state = 1
LOW state = 0

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

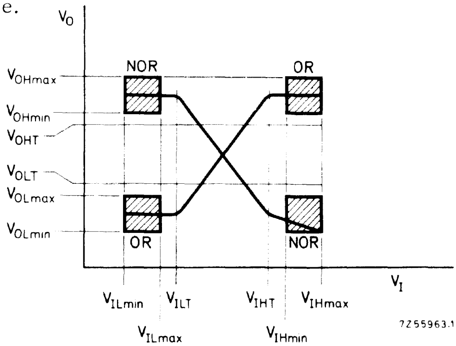
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2, 5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2, 0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0, 840	−0, 810	−0, 720	V
V_{IHT}	−1, 145	−1, 105	−1, 045	V
V_{ILT}	−1, 490	−1, 475	−1, 450	V
V_{ILmin}	−1, 870	−1, 850	−1, 830	V



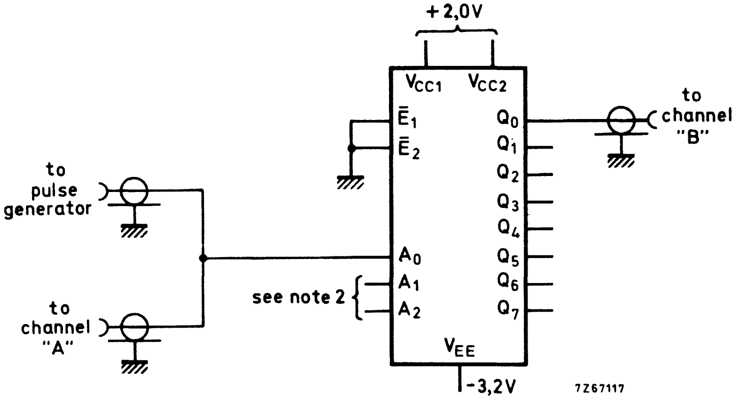
	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min.	−1000	−960	−900	mV	all inputs at V_{ILmin} for Q_0
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1, 870	−1, 850	−1, 830	V	one $\bar{E}$ input at V_{IHmax}; other $\bar{E}$ input at V_{ILmin}
		typ.	−	−1, 720	−	V	
		max.	−1, 665	−1, 650	−1, 625	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	one A input at V_{IHT} or V_{ILT}; other A inp. at V_{ILmin} or V_{IHmax} [1])
Output threshold voltage LOW	V_{OLT}	max.	−1, 645	−1, 630	−1, 605	V	one $\bar{E}$ input at V_{IHT}; other $\bar{E}$ input at V_{ILmin}
Input current HIGH	I_{IH}	max.	−	265	−	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	95	−	mA	All inputs at V_{ILmin}
		max.	−	125	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0, 25	−		

[1]) See also function table on page 3.

CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time	t_{pdr}	1,5	4,0	6,0	ns	See waveforms on page 6
Fall propagation delay time	t_{pdf}	1,5	4,0	6,0	ns	
Rise time	t_r	1,1	2,0	3,3	ns	
Fall time	t_f	1,1	2,0	3,3	ns	
Input capacitance (see note 1)	C_I	–	–	5	pF	reflection measurement

Switching times test circuit

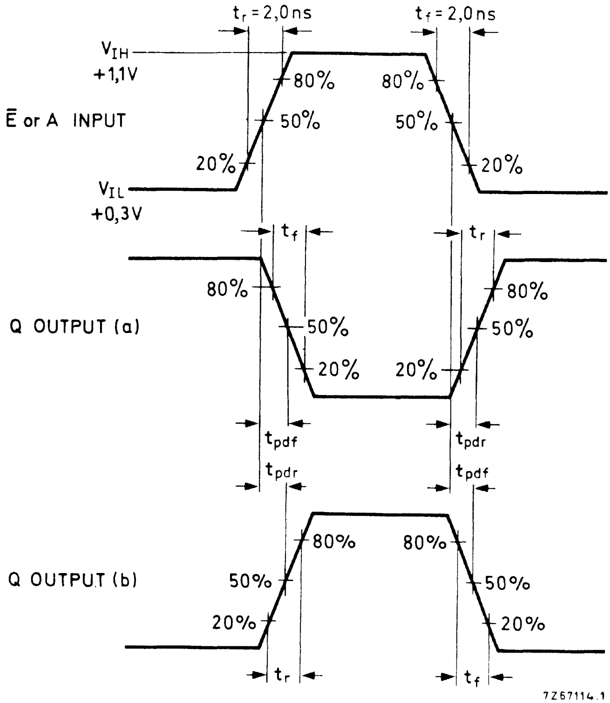


Notes

1. Input resistance is positive at any frequency.
2. Other A inputs are at +1,1 V or ground depending on output under test.
3. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.
5. Input impedance of the oscilloscope is 50 Ω.

CHARACTERISTICS (continued)

Switching times waveforms



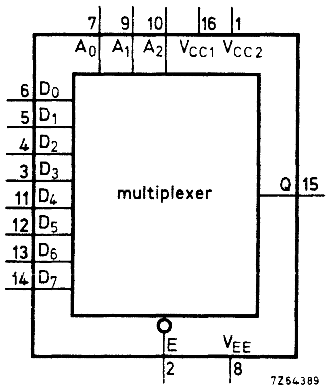
Output waveform (a) or (b) depending on particular input and output under test.

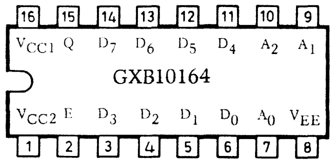
The GX family of CML silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

The GXB10164 performs 8-input multiplexing with enable input.
The output goes LOW when not enabled, thus permitting expansion of multiplexers by wired-ORing.

The GX family corresponds to the ECL 10 000series.

EIGHT INPUT MULTIPLEXER



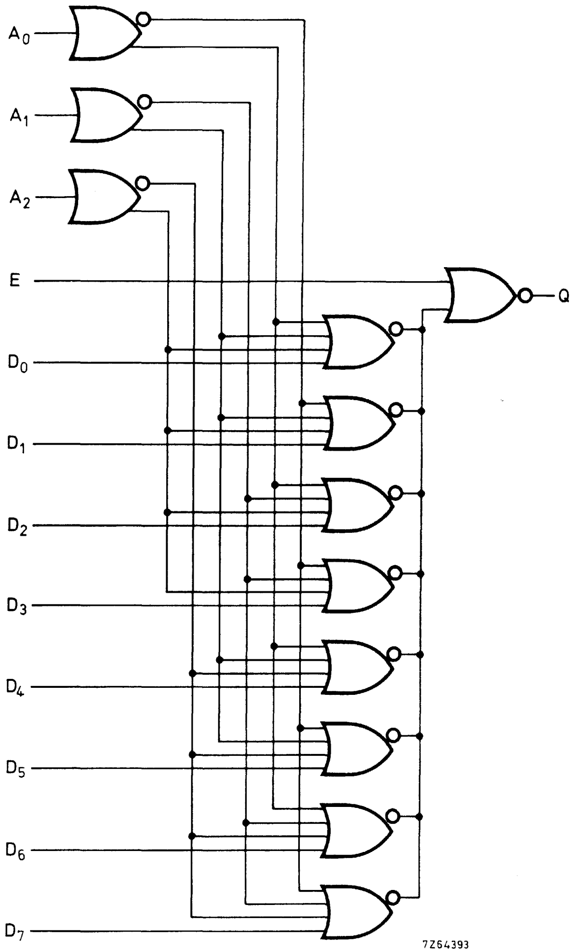


$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5,2$ V

QUICK REFERENCE DATA				
Supply voltage	V_{EE}		$-5,2 \pm 10\%$	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay	t_{pd}	typ.	3	ns
Output voltage HIGH state	V_{OH}	nom.	-880	mV
LOW state	V_{OL}	nom.	-1720	mV
Power consumption per package	P_{av}	typ.	310	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section)

LOGIC DIAGRAM



PIN NAMES

A_0 to A_2 : address inputs
D_0 to D_7 : data inputs
E : enable input

Note

Input pull-down resistors (50 kΩ) allow the unused inputs to be left open.

FUNCTION TABLE

inputs												output
A_0	A_1	A_2	$\overline{E}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
H	L	L	L	X	L	X	X	X	X	X	X	L
H	L	L	L	X	H	X	X	X	X	X	X	H
L	H	L	L	X	X	L	X	X	X	X	X	L
L	H	L	L	X	X	H	X	X	X	X	X	H
H	H	L	L	X	X	X	L	X	X	X	X	L
H	H	L	L	X	X	X	H	X	X	X	X	H
L	L	H	L	X	X	X	X	L	X	X	X	L
L	L	H	L	X	X	X	X	H	X	X	X	H
H	L	H	L	X	X	X	X	X	L	X	X	L
H	L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	L	X	X	X	X	X	X	L	X	L
L	H	H	L	X	X	X	X	X	X	H	X	H
H	H	H	L	X	X	X	X	X	X	X	L	L
H	H	H	L	X	X	X	X	X	X	X	H	H
X	X	X	H	X	X	X	X	X	X	X	X	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

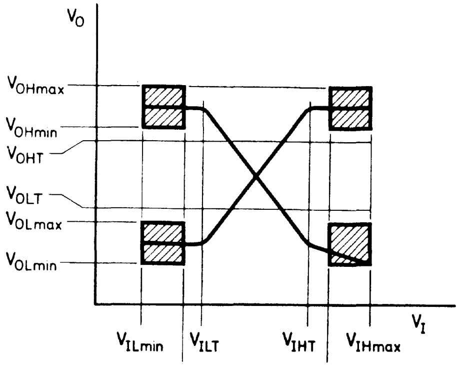
Supply voltage (d.c.)	V_{EE}	max.	−8,0	V
Input voltage	V_I		0 to V_{EE}	
Output current	I_O	max.	50	mA
Storage temperature	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; V_{EE} = −5, 2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow > 2, 5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2, 0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0	25	75	°C
V_{IHmax}	−0, 840	−0, 810	−0, 720	V
V_{IHT}	−1, 145	−1, 105	−1, 045	V
V_{ILT}	−1, 490	−1, 475	−1, 450	V
V_{ILmin}	−1, 870	−1, 850	−1, 830	V



	Symbol		T_{amb} (°C) 0	25	75		Conditions
Output voltage HIGH	V_{OH}	min	−1000	−960	−900	mV	D_0 at V_{IHmax} other inputs at V_{ILmin}
		typ.	−	−880	−	mV	
		max.	−840	−810	−720	mV	
Output voltage LOW	V_{OL}	min.	−1, 870	−1, 850	−1, 830	V	E at V_{IHmax} other inputs at V_{ILmin}
		typ.	−	−1, 720	−	V	
		max.	−1, 665	−1, 650	−1, 620	V	
Output threshold voltage HIGH	V_{OHT}	min.	−1020	−980	−920	mV	D_0 at V_{IHT} other inputs at V_{ILT}
Output threshold voltage LOW	V_{OLT}	max.	−1, 645	−1, 630	−1, 605	V	E at V_{IHT} other inputs at V_{ILT}
Input current HIGH	I_{IH}	max.	−	265	−	μA	V_{IHmax} for input under test
Input current LOW	I_{IL}	min.	−	10	−	μA	V_{ILmin} for input under test
Supply current	I_{EE}	typ.	−	60	−	mA	All inputs at V_{ILmin}
		max.	−	75	−	mA	
	$\frac{dV_{OL}}{dV_{EE}}$	typ.	−	0, 25	−		

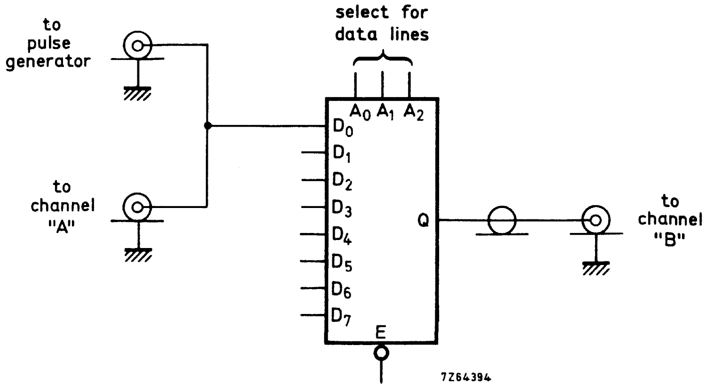
CHARACTERISTICS (a.c.) at V_{CC} = ground; V_{EE} = −5,2 V; T_{amb} = 25 °C

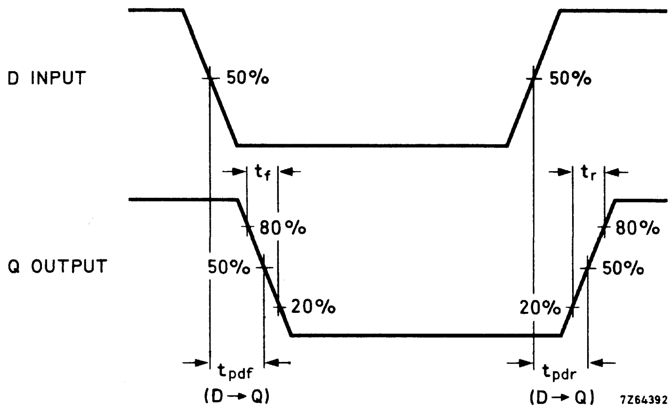
	Symbol	min.	typ.	max.		Conditions
Rise propagation delay time; (E → Q)	t_{pdr}	1,0	2,0	2,9	ns	See waveforms on page 6
Fall propagation delay time; (E → Q)	t_{pdf}	1,0	2,0	2,9	ns	
Rise propagation delay time; (A → Q)	t_{pdr}	2,0	4,0	6,0	ns	
Fall propagation delay time; (A → Q)	t_{pdf}	2,0	4,0	6,0	ns	
Rise propagation delay time; (D → Q)	t_{pdr}	1,5	3,0	4,5	ns	
Fall propagation delay time (D → Q)	t_{pdf}	1,5	3,0	4,5	ns	
Rise time	t_r	1,1	2,0	3,3	ns	
Fall time	t_f	1,1	2,0	3,3	ns	
Input capacitance (see note)	C_I	–	–	5	pF	reflection measurement

Note: Input resistance is positive at any frequency

CHARACTERISTICS (continued)

Switching times test circuits and waveforms



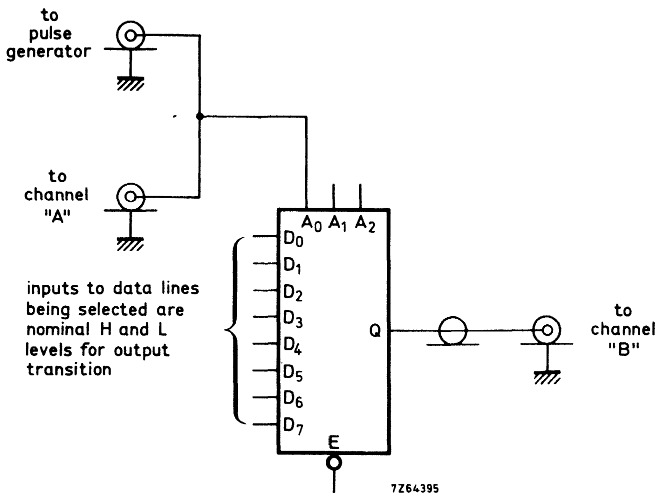


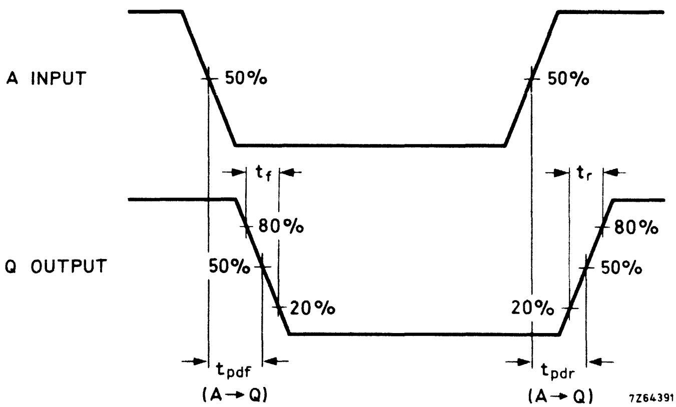
From data lines to output

Note

For conditions see page 8.

CHARACTERISTICS (continued)



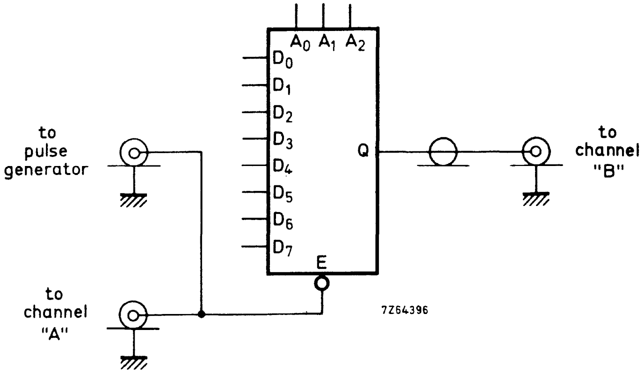


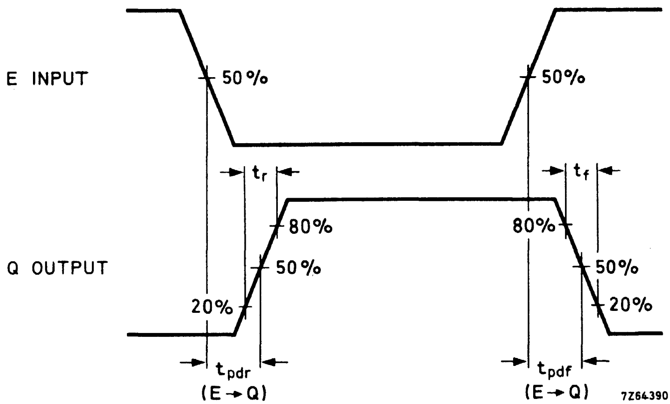
From address lines to output

Note

For conditions see page 8.

CHARACTERISTICS (continued)





From enable to output

Notes

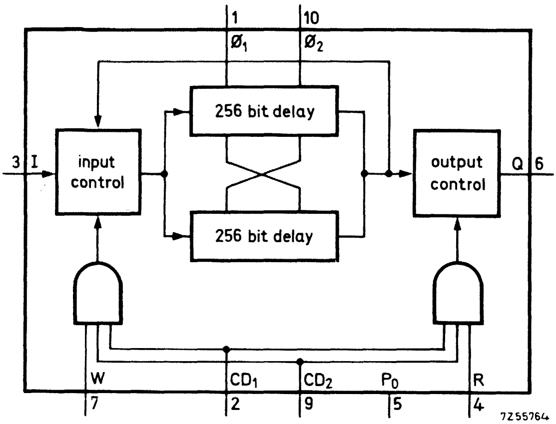
1. Input signal: $t_r = t_f = 2,0$ ns (20% to 80%); $V_{IH} = +1,1$ V; $V_{IL} = +0,3$ V.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.
5. $V_{CC} = +2,0$ V; $V_{EE} = -3,2$ V.

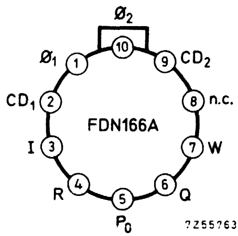
MOS FD family

FDN166A	512-bit recirculating dynamic SERIAL MEMORY (in TO-100)
FDN196A	dual 256-bit dynamic SHIFT REGISTER (in TO-100)
FDN196B	dual 256-bit dynamic SHIFT REGISTER (in 14 lead plastic DIL)
FDN216A	512-bit dynamic SHIFT REGISTER (in TO-100)
FDN216B	512-bit dynamic SHIFT REGISTER (in 14 lead plastic DIL)
FDN506	dual 32-bit static SHIFT REGISTER (in 14 lead metal ceramic DIL)
FDN536A	dual 100-bit static SHIFT REGISTER (in TO-100)
FDR116Z	READ-ONLY memory, 512 word, 5-bits per word (bit pattern to customer's specification)
FDR116Z1	READ-ONLY memory, 512 word, 5-bits per word (with fixed bit pattern for alpha numerical 5 x 7 dot code matrix character generator)
FDR116Z2	CHARACTER GENERATOR (5 x 7 dot matrix; row scan system)
FDR126Z	READ-ONLY memory, 256 word, 10-bits per word (bit pattern to customer's specification)
FDR126Z1	READ-ONLY memory, 256 word, 10-bits per word (with fixed bit pattern for conversion from ASCII to selectric line code and vica versa)
FDR131Z	READ-ONLY memory, 512 word, 8-bits per word (bit pattern to customer's specification)
FDR131Z1	READ-ONLY memory, 512 word, 8-bits per word (with fixed bit pattern for conversion from ASCII to EBCDIC code and vica versa)
FDR131Z2	CHARACTER GENERATOR (5 x 7 dot matrix; column scan system)
FDR146(B)Z	READ-ONLY memory, 512 word, 10-bits per word (bit pattern to customer's specification)
FDR146(B)Z1	STATIC CHARACTER GENERATOR HIGH RESOLUTION UPPER CASE (7 x 9 dot matrix, column scan system)
FDR146(B)Z2	CHARACTER GENERATOR upper and lower case (5 x 7 dot matrix; row scan system)
FDR151(B)Z	STATIC READ ONLY MEMORY 2048 words, 8-bits per word

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

512-BIT RECIRCULATING DYNAMIC SERIAL MEMORY





P_0 connected to the metal case

QUICK REFERENCE DATA						
Clock rate	f_ϕ	0,005	to	5	MHz
Data rate	f_D	0,01	to	5	MHz
Power consumption per bit					
at 1 MHz data rate	P_{av}	0,07			mW
at 5 MHz data rate	P_{av}	0,35			mW
Operating ambient temperature	T_{amb}	−55	to	+85	^oC

PACKAGE OUTLINE : TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN166A consists of two 256-bit 2-phase dynamic shift registers, with internal multiplexing and recirculation circuitry. [1])
Data is written into and read from the device at both ϕ_1 and ϕ_2, so that the data rate is twice the clock rate. The chip disable (CD) inputs allow selection of one-out-of--many circuits in larger memories. Both CD inputs have to be in the HIGH state to activate the device. Data will be written in when W, CD_1, and CD_2 are in the HIGH state; at all other times the device is in the recirculation mode. The output is active only when R, CD_1 and CD_2 are in the HIGH state; so that the outputs of more devices can be wired-OR.
With the FDN166A large serial memories with a drum-like organisation can be made.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0		+0,5 to	−30	V
Power dissipation	P_{tot}	max.	625	mW
Junction temperature up to T_{amb} = 25 °C	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	200	°C/W

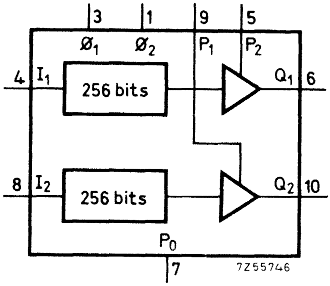
Note
All terminals are protected against over-voltage due to static charges.

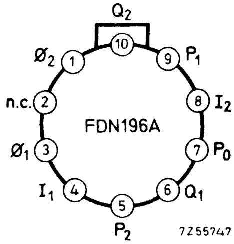
[1]) External behaviour: 512-bit shift register.

FDN196A
FDN196B

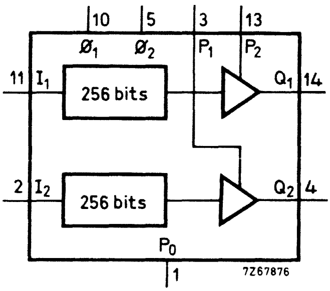
The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enchancement mode technology.

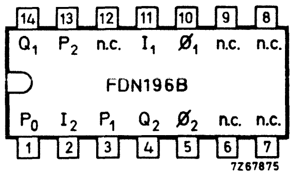
DUAL 256-BIT DYNAMIC SHIFT REGISTER





P_0 connected to metal case





QUICK REFERENCE DATA				
Clock rate	f_ϕ		0,01 to 3	MHz
Power consumption per bit at f_ϕ = 3 MHz	P_{av}	typ.	0,36	mW
Operating ambient temperature FDN196A:	T_{amb}		−55 to +85	°C
FDN196B:	T_{amb}		0 to +70	°C
D.C. noise margin	$M_H;M_L$	>	1	V

PACKAGE OUTLINE

FDN196A : TO-100 (See General Section)
FDN196B : 14 lead plastic dual in-line (type A) (See General Section)

GENERAL DESCRIPTION

The FDN196A(B) consists of two 256-bit 2-phase dynamic shift registers, with common clock lines.
The device has two low impedance push-pull output buffers, with separate supply voltages. Thus the two outputs may be independently biased to drive a bipolar load or other MOS circuits.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0 +0,5 to −30 V

		FDN196A	FDN196B	
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max. 625	550	mW
Junction temperature	T_j	max. 150	135	°C
Storage temperature	T_{stg}	−65 to +150	−65 to +150	°C
Total current through terminals P_1, P_2	$-I_{P1}$, $-I_{P2}$	max. 20	20	mA
Output current (per output)	$\pm I_Q$	max. 20	20	mA

THERMAL RESISTANCE

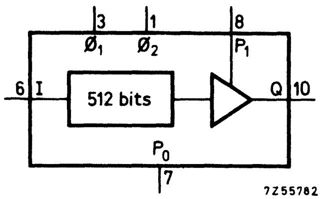
		FDN196A	FDN196B	
From junction to ambient	$R_{th\ j-a}$	= 200	225	°C/W

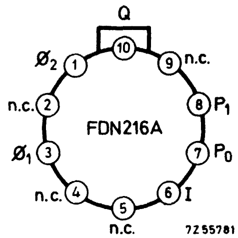
Note

All terminals are protected against over-voltage caused by static charges.

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

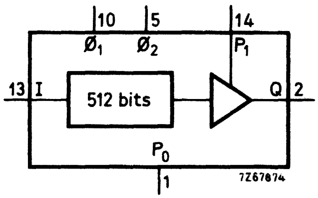
512-BIT DYNAMIC SHIFT REGISTER

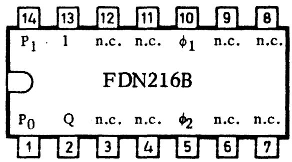




top view

P_0 connected to the metal case





QUICK REFERENCE DATA				
Clock rate	f_ϕ		0,01 to 3	MHz
Power consumption per bit at f_ϕ = 3 MHz	P_{av}	typ.	0,36	mW
Operating ambient temperature				
FDN216A :	T_{amb}		−55 to +85	°C
FDN216B :	T_{amb}		0 to +70	°C
D.C. noise margin	M_H; M_L	>	1	V

PACKAGE OUTLINE

FDN216A: TO-100 (See General Section).
FDN216B: 14 lead plastic dual in-line (Type A) (See General Section).

GENERAL DESCRIPTION

The FDN216A(B) is a 512-bit 2-phase dynamic shift register.
The device has a low impedance push-pull output buffer.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0 +0,5 to −30 V

		FDN216A	FDN216B	
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max. 625	550	mW
Junction temperature	T_j	max. 150	135	°C
Storage temperature	T_{stg}	−65 to +150	−55 to +150	°C
Total current through terminal P_1	$-I_{P1}$	max. 20	20	mA
Output current (per output)	$\pm I_Q$	max. 20	20	mA

THERMAL RESISTANCE

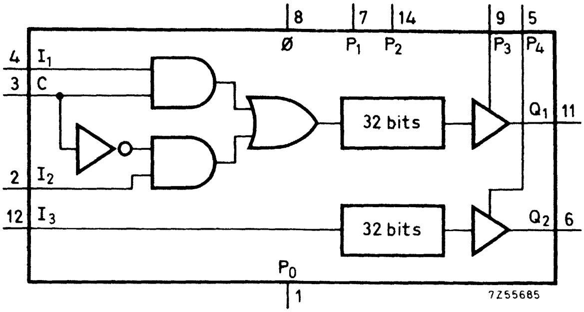
		FDN216A	FDN216B	
From junction to ambient	$R_{th\ j-a}$	= 200	225	°C/W

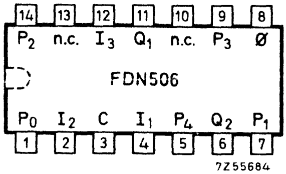
Note

All terminals are protected against over-voltage caused by static charges.

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

DUAL 32-BIT STATIC REGISTER





P_0 connected to the metal bottom

QUICK REFERENCE DATA				
Supply voltages	V_{P1}		−24 to −28	V
	V_{P2}		−12 to −14	V
Clock frequency	f_ϕ		0 to 1,5	MHz
Power consumption per bit at f_ϕ = 1,5 MHz	P_{av}	typ.	2	mW
Operating ambient temperature	T_{amb}		−55 to +85	°C
D.C. noise margin	M_H, M_L	>	1	V

PACKAGE OUTLINE 14 lead metal ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDN506 is a dual 32-bit static registers. It requires a single phase, low voltage, external clock, and be operated down to d.c. without loss of stored information.
The device utilizes common power and clock lines; the output buffer supplies are separated to facilitate independent biasing for MOS or TTL load drive.
The FDN506 contains the gating, external SELECT command and data inputs for selection of two independent data streams.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

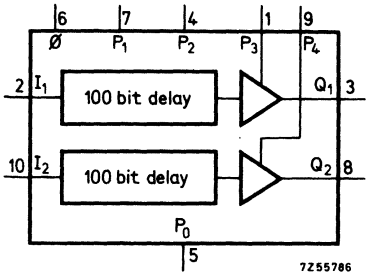
Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0,5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	800	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminals P_3, P_4	$-I_{P3}, -I_{P4}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

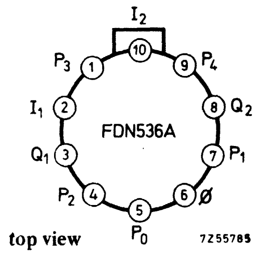
THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	156	°C/W

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

DUAL 100-BIT STATIC SHIFT REGISTER





P_0 connected to the metal case

QUICK REFERENCE DATA				
Clock rate	f_{ϕ}		0 to 1,5	MHz
Supply voltages	V_{P1}		−24 to −28	V
	$V_{P2}; V_{P3}; V_{P4}$		−12 to −14	V
Power consumption per bit at f_{ϕ} = 1,5 MHz	P_{av}	typ.	1	mW
Operating ambient temperature	T_{amb}		−55 to +85	°C
D.C. noise margin	M_H, M_L	>	1	V

PACKAGE OUTLINE TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN536A is a monolithic dual 100-bit shift register. The two shift registers have each one serial input and output. They operate from common clocks and supply lines.
The device has low impedance push-pull output buffers, which, when appropriately biased, are capable of interfacing direct with MOS, TTL, DTL and other loads.
The buffer supply terminals P_3 and P_4 are separate supplies which determine the output LOW signals only. This provides an output level that is independent of supply voltages V_{P1}, V_{P2}, the amplitude and width of the clock pulses.
All inputs, outputs, supply terminals and clock inputs are protected against over-voltage caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

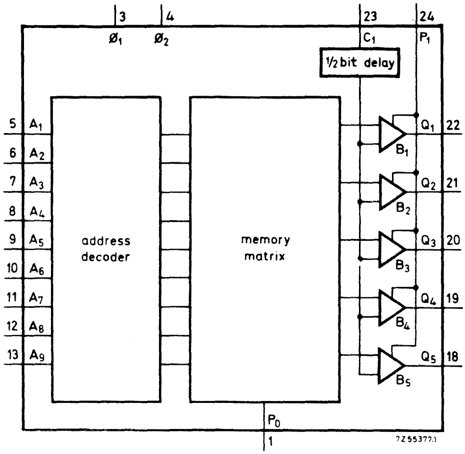
Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0,5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminals P_2, P_3 and P_4	$-I_{P2}$; $-I_{P3}$; $-I_{P4}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

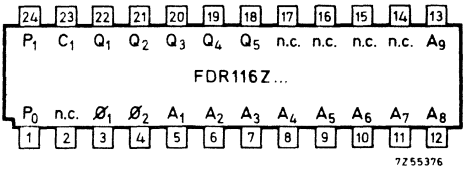
THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	200	°C/W

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ ONLY MEMORY, 512 WORD, 5 BITS PER WORD





QUICK REFERENCE DATA				
Read access time	t_{AR}	max.	850	ns
Clock rate	f_{ϕ}	max.	1.2	MHz
Power dissipation at f_{ϕ} = 1 MHz	P_{ϕ}	typ.	90	mw
D.C. noise margin	M_L, M_H	>	1	V
Operating ambient temperature	T_{amb}	−55 to +85		°C

PACKAGE OUTLINE 24 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDR116Z is a monolithic 2560 bit read only memory. When ordering an FDR116Z the customer must send a bit pattern matrix with the desired content. For performance evaluation, we can supply specimens of FDR116Z1, which is identical to the FDR116Z but contains a bit pattern of our own. The FDR116Z requires a two phase clock, but the outputs remain steady as long as the address remains unchanged. The normal configuration is as a 512 word, 5 bits per word, parallel output ROM. An output inhibit control allows the use of multiple FDR116Z in a wired-OR configuration.
The memory matrix is programmed with the aid of a mask pattern during manufacture. The only d.c. supply is the output buffer supply, which is variable and can be biased to drive bipolar output loads direct.
The patterns permanently stored in the memory matrix of the FDR116Z1 are described in the following data sheets.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0.5 to	−30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminal P_2	$-I_{P2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C

ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0.1	–	1.2 MHz	see note
Clock pulse width	$t_{\phi 1L}$ $t_{\phi 2L}$	0.50 0.25	– –	1.0 μs 1.0 μs	see timing diagram for parameter definitions
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10 μs	see note
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10 μs	
Clock delay time	$t_{\phi 1 \phi 2}$	0	–	4.5 μs	
Clock delay time	$t_{\phi 2 \phi 1}$	0	–	4.5 μs	
Clock input voltage level HIGH LOW	 $V_{\phi H}$ $V_{\phi L}$	 −2 −28	 0 −26	 +0.3 V −24 V	
Address input and output inhibit input logic levels: HIGH LOW	 V_{AH}, V_{CH} V_{AL}, V_{CL}	 −2 −14	 0 −12	 +0.3 V −9 V	

Note

At frequencies higher than 870 kHz, $t_{\phi 1Lmax}$ and $t_{\phi 2Lmin}$ will be determined by $t_{\phi LHmax}$ and $t_{\phi HLmax}$.

CHARACTERISTICS

Test conditions: V_{P_1} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded;
standard load: 30 pF in parallel with 150 kΩ to P_0.

ELECTRICAL DATA	Symbol	min.	typ.	max.	Conditions and references
Read access time	t_{AR}	-	750	850 ns	see note 1
Output levels:					
HIGH	V_{QH}	-1	-	0 V	
LOW	V_{QL}	-14	-	-10 V	
Address input capacitance	C_A	-	3.2	4.0 pF	bias: V_A = 0 V; f_ϕ = 1 MHz
Output inhibit input capacitance	C_C	-	3.2	4.0 pF	bias: V_C;V_ϕ = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$	-	21	30 pF	bias: V_C;V_ϕ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	-	13	18 pF	bias: V_C;V_ϕ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 1}$	-	13	18 pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	-	7.4	10 pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Leakage currents:					
Address input and output inhibit input currents	$-I_{AL}$, $-I_{CL}$	-	-	1 μA	V_A = V_C = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	-	-	100 μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance					
HIGH	R_{QH}	-	300	- Ω	
LOW	R_{QL}	-	170	- Ω	V_{P_1} = −5 V
Clock power dissipation (see note 2)	P_ϕ	-	36	- mW	f_ϕ = 1 MHz
Input current (see note 3)	$-I_{P_1}$	-	4.0	- mA	V_{P1} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:					
fall time	t_{THL}	-	100	- ns	
rise time	t_{TLH}	-	100	- ns	
Delay times: fall time	t_{DHL}	-	20	- ns	
rise time	t_{DLH}	-	20	- ns	
D.C. noise margin	M_L, M_H	1	-	- V	

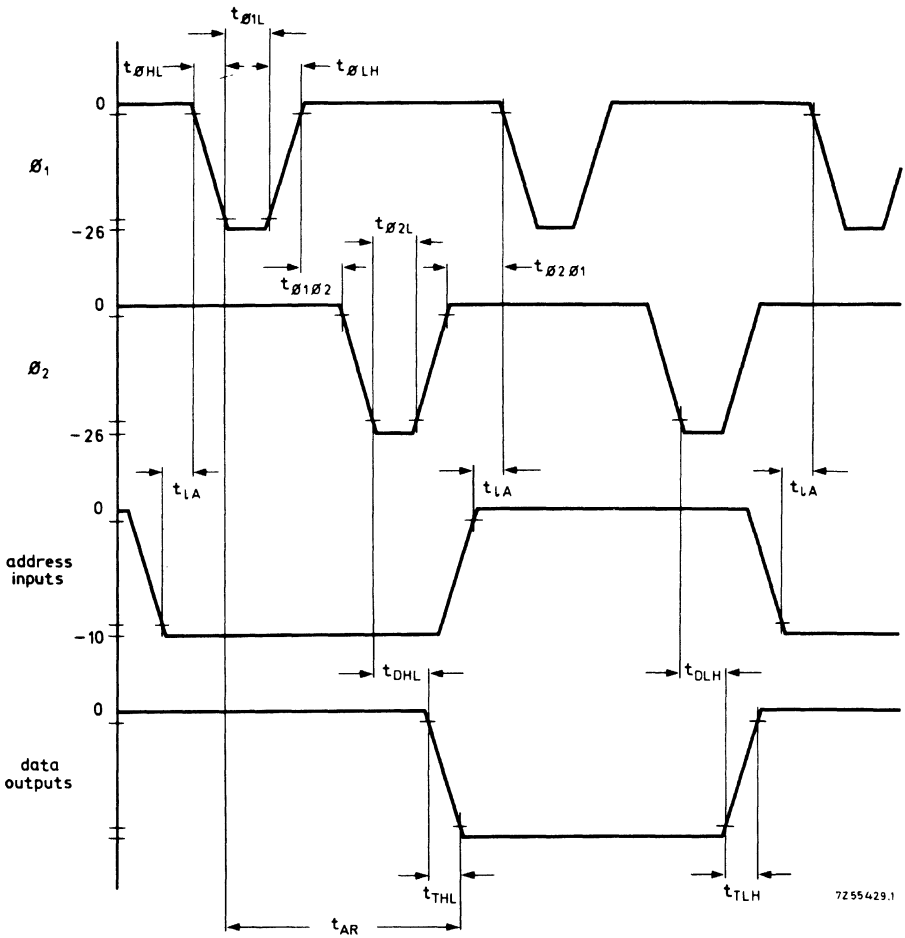
Note 1: The minimum access time assumes the summation of the rise time of ϕ_1 and the fall time of ϕ_2 is less than 40 ns.

Note 2: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 3: I_{P_1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Note

The indicated points on the vertical axis are specified in the glossary of terms.

Address and output inhibit timing requirements:

1. Address input (and output inhibit input) signals are clocked into the memory during ϕ_1, and must remain present throughout ϕ_1. Address lead time ($t_{\ell A}$) must be ≥ 0.
2. The output signals remain steady **for as many clock cycles as the address and output** inhibit signals remain unchanged.

CHARACTERISTICS (continued)

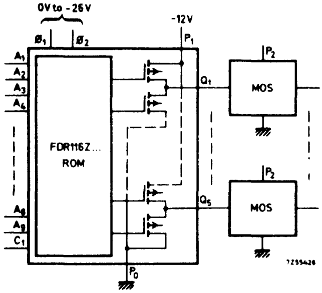
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Fall delay time: t_{DHL}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Read access time: t_{AR}
   The time between the 90% point on the negative going edge of the clock pulse ϕ_1 and the time at which the output is present, defined at 90%.

OUTPUT BUFFER DESCRIPTION

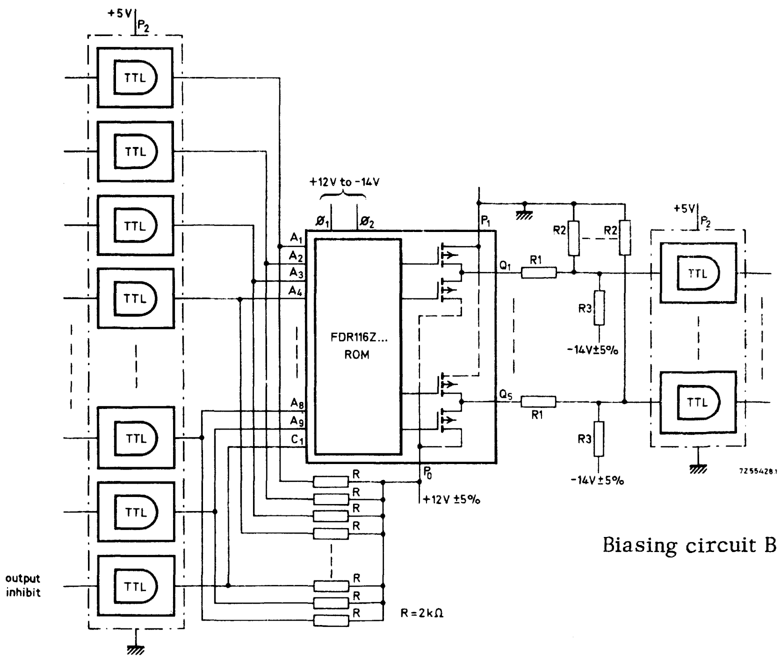
The only d.c. supply required is V_{P1}, the push-pull output buffer supply. V_{P1} may be varied between 0 and −28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A.

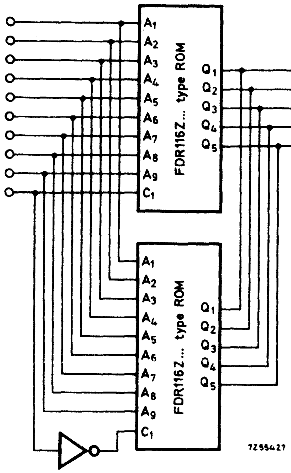
2. Biasing circuit B may be used to interface with TTL, both at the input and the output of the ROM. Note that no active interface devices are required. At the address and C inputs any TTL devices can be used that will sustain a minimum of +12 V at their output terminals.



Biasing circuit B.

WIRED-OR APPLICATIONS

Use of wired-or output capability:
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-OR with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. This output inhibit wired-OR capability makes it possible to use the FDR116Z type ROM in many different applications, such as the one shown here.



1024 words, 5 bits per word ROM

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 12. Eight forms are needed for 512 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched card are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customers's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS

   a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is bit 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.

   b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.

   c) Bit 7, 8 and 9 specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1])
   Memories of 512 words need 8 pages, of specifications.

   d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form.

[1]) See example on page 12

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN (continued)

2. CONTENTS (DATA OUTPUTS)

   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 5 using only ones (1 = LOW) and zeros (0 = HIGH).

3. AUTHORIZED SIGNATURE

   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

CHARACTER GENERATION

The FDR116Z1 is meant for generating ASCII characters for display in a system in which each character is made up of seven 5-bit rows that are traced one at a time. It is capable of storing 64 different characters, each having its own 6-bit address.

To generate a line of characters for display, word addresses are applied in sequence to the WORD SELECT inputs A_1 to A_3 and character addresses to the CHARACTER SELECT inputs A_4 to A_9. First, the row to be traced is selected by applying its address (3 bits) to inputs A_1 to A_3; then the desired characters are selected by applying their addresses (6 bits each) to inputs A_4 to A_9. When one row in a line of characters has been traced, the next row is generated by applying a new word address (inputs A_1 to A_3) and repeating the same sequence of character addresses as before. After the sequence of character addresses has been repeated in conjunction with the word addresses for all seven rows, the full line of characters has been generated. Of the FDR116Z1, a selection is available, which has a maximum read rating of 1.67 MHz (cycle time 600 ns).

PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern FDR 116 . . .

page of

AUTHORIZED SIGNATURE

CUSTOMER NAME:

DATE

ADDRESS INPUTS 9 8 7 6 5 4 3 2 1	CONTENTS 00 OUTPUTS 10 9 8 7 6 5 4 3 2 1	01 OUTPUTS 10 9 8 7 6 5 4 3 2 1	10 OUTPUTS 10 9 8 7 6 5 4 3 2 1	11 OUTPUTS 10 9 8 7 6 5 4 3 2 1
XX0000				
XX0001				
XX0010				
XX0011				
XX0100				
XX0101				
XX0110				
XX0111				
XX1000				
XX1001				
XX1010				
XX1011				
XX1100				
XX1101				
XX1110				
XX1111				

Note: 1 = LOW; 0 = HIGH

ASCII CHARACTER ADDRESS INPUTS A9 A8 A7 A6 A5 A4	WORD SELECT INPUTS A3 A2 A1	OUTPUTS Q5 Q4 Q3 Q2 Q1 00	OUTPUTS Q5 Q4 Q3 Q2 Q1 01	OUTPUTS Q5 Q4 Q3 Q2 Q1 10	OUTPUTS Q5 Q4 Q3 Q2 Q1 11
0 0 0 X X 0	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	0 1 1 1 0	1 1 1 1 0	1 1 1 1 0	1 1 1 1 1
	0 1 0	1 0 0 0 1	1 0 0 0 1	1 0 0 0 1	1 0 0 0 0
	0 1 1	1 0 1 0 1	1 0 0 0 1	1 0 0 0 1	1 0 0 0 0
	1 0 0	1 0 1 1 1	1 1 1 1 0	1 0 0 0 1	1 1 1 1 0
	1 0 1	1 0 1 1 0	1 0 0 0 1	1 0 0 0 1	1 0 0 0 0
	1 1 0	1 0 0 0 0	1 0 0 0 1	1 0 0 0 1	1 0 0 0 0
	1 1 1	0 1 1 1 1	1 1 1 1 0	1 1 1 1 0	1 0 0 0 0
0 0 0 X X 1	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	0 0 1 0 0	0 1 1 1 0	1 1 1 1 1	0 1 1 1 1
	0 1 0	0 1 0 1 0	1 0 0 0 1	1 0 0 0 0	1 0 0 0 0
	0 1 1	1 0 0 0 1	1 0 0 0 0	1 0 0 0 0	1 0 0 0 0
	1 0 0	1 0 0 0 1	1 0 0 0 0	1 1 1 1 0	1 0 0 0 0
	1 0 1	1 1 1 1 1	1 0 0 0 0	1 0 0 0 0	1 0 0 1 1
	1 1 0	1 0 0 0 1	1 0 0 0 1	1 0 0 0 0	1 0 0 0 1
	1 1 1	1 0 0 0 1	0 1 1 1 0	1 1 1 1 1	0 1 1 1 1
0 0 1 X X 0	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	1 0 0 0 1	0 0 0 0 1	1 0 0 0 0	1 0 0 0 1
	0 1 0	1 0 0 0 1	0 0 0 0 1	1 0 0 0 0	1 0 0 0 1
	0 1 1	1 0 0 0 1	0 0 0 0 1	1 0 0 0 0	1 1 0 0 1
	1 0 0	1 1 1 1 1	0 0 0 0 1	1 0 0 0 0	1 0 1 0 1
	1 0 1	1 0 0 0 1	0 0 0 0 1	1 0 0 0 0	1 0 0 1 1
	1 1 0	1 0 0 0 1	1 0 0 0 1	1 0 0 0 0	1 0 0 0 1
	1 1 1	1 0 0 0 1	0 1 1 1 0	1 1 1 1 1	1 0 0 0 1
0 0 1 X X 1	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	0 1 1 1 0	1 0 0 0 1	1 0 0 0 1	0 1 1 1 0
	0 1 0	0 0 1 0 0	1 0 0 1 0	1 1 0 1 1	1 0 0 0 1
	0 1 1	0 0 1 0 0	1 0 1 0 0	1 0 1 0 1	1 0 0 0 1
	1 0 0	0 0 1 0 0	1 1 0 0 0	1 0 1 0 1	1 0 0 0 1
	1 0 1	0 0 1 0 0	1 0 1 0 0	1 0 0 0 1	1 0 0 0 1
	1 1 0	0 0 1 0 0	1 0 0 1 0	1 0 0 0 1	1 0 0 0 1
	1 1 1	0 1 1 1 0	1 0 0 0 1	1 0 0 0 1	0 1 1 1 0

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
A9 A8 A7 A6 A5 A4	A3 A2 A1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1
x x →		00	01	10	11
0 1 0 x x 0	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	1 1 1 1 0	1 1 1 1 0	1 1 1 1 1	1 0 0 0 1
	0 1 0	1 0 0 0 1	1 0 0 0 1	0 0 1 0 0	1 0 0 0 1
	0 1 1	1 0 0 0 1	1 0 0 0 1	0 0 1 0 0	1 0 0 0 1
	1 0 0	1 1 1 1 0	1 1 1 1 0	0 0 1 0 0	1 0 0 0 1
	1 0 1	1 0 0 0 0	1 0 1 0 0	0 0 1 0 0	1 0 0 0 1
	1 1 0	1 0 0 0 0	1 0 0 1 0	0 0 1 0 0	0 1 0 1 0
	1 1 1	1 0 0 0 0	1 0 0 0 1	0 0 1 0 0	0 0 1 0 0
0 1 0 x x 1	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	0 1 1 1 0	0 1 1 1 0	1 0 0 0 1	1 0 0 0 1
	0 1 0	1 0 0 0 1	1 0 0 0 1	1 0 0 0 1	1 0 0 0 1
	0 1 1	1 0 0 0 1	1 0 0 0 0	1 0 0 0 1	1 0 0 0 1
	1 0 0	1 0 0 0 1	0 1 1 1 0	1 0 0 0 1	1 0 1 0 1
	1 0 1	1 0 1 0 1	0 0 0 0 1	1 0 0 0 1	1 0 1 0 1
	1 1 0	1 0 0 1 0	1 0 0 0 1	1 0 0 0 1	1 1 0 1 1
	1 1 1	0 1 1 0 1	0 1 1 1 0	0 1 1 1 0	1 0 0 0 1
0 1 1 x x 0	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	1 0 0 0 1	1 1 1 1 1	0 0 0 0 0	0 0 0 0 0
	0 1 0	1 0 0 0 1	0 0 0 0 1	1 0 0 0 0	0 0 0 0 0
	0 1 1	0 1 0 1 0	0 0 0 1 0	0 1 0 0 0	0 0 1 0 0
	1 0 0	0 0 1 0 0	0 0 1 0 0	0 0 1 0 0	0 1 0 1 0
	1 0 1	0 1 0 1 0	0 1 0 0 0	0 0 0 1 0	1 0 0 0 1
	1 1 0	1 0 0 0 1	1 0 0 0 0	0 0 0 0 1	0 0 0 0 0
	1 1 1	1 0 0 0 1	1 1 1 1 1	0 0 0 0 0	0 0 0 0 0
0 1 1 x x 1	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	1 0 0 0 1	1 1 1 1 1	1 1 1 1 1	0 0 0 0 0
	0 1 0	1 0 0 0 1	1 1 0 0 0	0 0 0 1 1	0 0 0 0 0
	0 1 1	0 1 0 1 0	1 1 0 0 0	0 0 0 1 1	0 0 0 0 0
	1 0 0	0 0 1 0 0	1 1 0 0 0	0 0 0 1 1	0 0 0 0 0
	1 0 1	0 0 1 0 0	1 1 0 0 0	0 0 0 1 1	0 0 0 0 0
	1 1 0	0 0 1 0 0	1 1 0 0 0	0 0 0 1 1	0 0 0 0 0
	1 1 1	0 0 1 0 0	1 1 1 1 1	1 1 1 1 1	1 1 1 1 1

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
A9 A8 A7 A6 A5 A4	A3 A2 A1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1
X X →		00	01	10	11
1 0 0 X X 0	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	0 0 0 0 0	0 1 0 1 0	0 0 1 0 0	0 1 0 0 0
	0 1 0	0 0 0 0 0	0 1 0 1 0	0 1 1 1 1	1 0 1 0 0
	0 1 1	0 0 0 0 0	0 1 0 1 0	1 0 1 0 0	1 0 1 0 0
	1 0 0	0 0 0 0 0	0 0 0 0 0	0 1 1 1 0	0 1 0 0 0
	1 0 1	0 0 0 0 0	0 0 0 0 0	0 0 1 0 1	1 0 1 0 1
	1 1 0	0 0 0 0 0	0 0 0 0 0	1 1 1 1 0	1 0 0 1 0
	1 1 1	0 0 0 0 0	0 0 0 0 0	0 0 1 0 0	0 1 1 0 1
1 0 0 X X 1	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	0 0 1 0 0	0 1 0 1 0	1 1 0 0 0	0 0 1 0 0
	0 1 0	0 0 1 0 0	0 1 0 1 0	1 1 0 0 1	0 0 1 0 0
	0 1 1	0 0 1 0 0	1 1 1 1 1	0 0 0 1 0	0 0 1 0 0
	1 0 0	0 0 1 0 0	0 1 0 1 0	0 0 1 0 0	0 0 0 0 0
	1 0 1	0 0 1 0 0	1 1 1 1 1	0 1 0 0 0	0 0 0 0 0
	1 1 0	0 0 0 0 0	0 1 0 1 0	1 0 0 1 1	0 0 0 0 0
	1 1 1	0 0 1 0 0	0 1 0 1 0	0 0 0 1 1	0 0 0 0 0
1 0 1 X X 0	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	0 0 0 1 0	0 0 1 0 0	0 0 0 0 0	0 0 0 0 0
	0 1 0	0 0 1 0 0	1 0 1 0 1	0 0 0 0 0	0 0 0 0 0
	0 1 1	0 1 0 0 0	0 1 1 1 0	0 0 0 0 0	0 0 0 0 0
	1 0 0	0 1 0 0 0	0 0 1 0 0	0 0 0 0 0	0 0 0 0 0
	1 0 1	0 1 0 0 0	0 1 1 1 0	0 0 1 0 0	0 0 0 0 0
	1 1 0	0 0 1 0 0	1 0 1 0 1	0 0 1 0 0	0 0 0 0 0
	1 1 1	0 0 0 1 0	0 0 1 0 0	0 1 0 0 0	0 0 1 0 0
1 0 1 X X 1	0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 0 1	0 0 1 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
	0 1 0	0 0 0 1 0	0 0 1 0 0	0 0 0 0 0	0 0 0 0 1
	0 1 1	0 0 0 0 1	0 0 1 0 0	0 0 0 0 0	0 0 0 1 0
	1 0 0	0 0 0 0 1	1 1 1 1 1	1 1 1 1 1	0 0 1 0 0
	1 0 1	0 0 0 0 1	0 0 1 0 0	0 0 0 0 0	0 1 0 0 0
	1 1 0	0 0 0 1 0	0 0 1 0 0	0 0 0 0 0	1 0 0 0 0
	1 1 1	0 0 1 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
A9 A8 A7 A6 A5 A4	A3 A2 A1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1
X X →		00	01	10	11
1 1 0 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 0 0 1 1 1 0 1 0 1 1 1 0 0 1 1 0 0 0 1 0 1 1 1 0	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 0 0 0 0 1 0 0 1 1 0 0 1 0 0 0 1 0 0 0 0 1 1 1 1 1	0 0 0 0 0 0 0 0 1 0 0 0 1 1 0 0 1 0 1 0 1 0 0 1 0 1 1 1 1 1 0 0 0 1 0 0 0 0 1 0	0 0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 0 0 0 0 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 0 1 1 1 0
1 1 0 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 0 0 1 0 0 0 1 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 1 1 0	0 0 0 0 0 1 1 1 1 1 0 0 0 0 1 0 0 0 1 0 0 0 1 1 0 0 0 0 0 1 1 0 0 0 1 0 1 1 1 0	0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 0 1 0 0 0 0 1 1 0 0 0 1 0 1 1 1 0	0 0 0 0 0 1 1 1 1 1 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0
1 1 1 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 0 1 1 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 1 0	0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0
1 1 1 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 0 1 1 1 1 0 0 0 0 1 0 0 0 1 0 1 1 1 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0

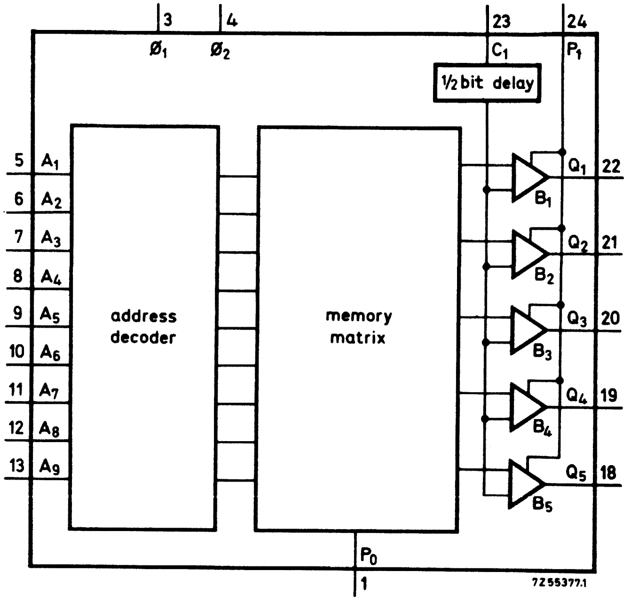
ROM ORGANISATION

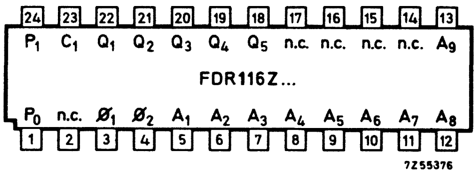
In this example, with the word select input address fixed, the ASCII character addresses are sequentially altered to produce one line of three different characters, left to right. After 8 sequential binary word select iterations using the same character address sequence, the complete line of characters is formed, including a SPACE line.

A_3 A_2 A_1 word select inputs		ASCII character address for R applied to A_4 to A_9 0 1 0 0 1 0	ASCII character address for O applied to A_4 to A_9 0 0 1 1 1 1	ASCII character address for M applied to A_4 to A_9 0 0 1 1 0 1
0 0 0	row_1	→ 0 0 0 0 0	→ 0 0 0 0 0	→ 0 0 0 0 0
0 0 1	row_2	→ 1 1 1 1 0	→ 0 1 1 1 0	→ 1 0 0 0 1
0 1 0	row_3	→ 1 0 0 0 1	→ 1 0 0 0 1	→ 1 1 0 1 1
0 1 1	row_4	→ 1 0 0 0 1	→ 1 0 0 0 1	→ 1 0 1 0 1
1 0 0	row_5	→ 1 1 1 1 0	→ 1 0 0 0 1	→ 1 0 1 0 1
1 0 1	row_6	→ 1 0 1 0 0	→ 1 0 0 0 1	→ 1 0 0 0 1
1 1 0	row_7	→ 1 0 0 1 0	→ 1 0 0 0 1	→ 1 0 0 0 1
1 1 1	row_8	→ 1 0 0 0 1	→ 0 1 1 1 0	→ 1 0 0 0 1

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

CHARACTER GENERATOR
(5 × 7DOT MATRIX; ROW SCAN SYSTEM)





P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA				
Read acces time	t_{AR}	max.	850	ns
Clock rate	f_ϕ	max.	1.2	MHz
Power dissipation at f_ϕ = 1 MHz	P_ϕ	typ.	90	mW
D.C. noise margin	M_L, M_H	>	1	V
Operating ambient temperature	T_{amb}	−55 to +85		°C

PACKAGE OUTLINE 24 lead metal-ceramic dual in-line (See General Section).

GENERAL DESCRIPTION

The FDR116Z2 is a pre-programmed specimen of the FDR116Z.
It is intended for use as character generator in display systems, using a 5 x 7 dot matrix, where the characters are built-up with one horizontal row at a time.
The device contains a sub-set of the ASCII character set viz. the lower case symbols and a pictorial representation of the control symbols.
When the device is used in combination with the FDR116Z1, the full 7-bit ASCII code character set can be displayed.

RATINGS

CHARACTERISTICS

OUTPUT BUFFER DESCRIPTION

For this information see data sheets of FDR116Z

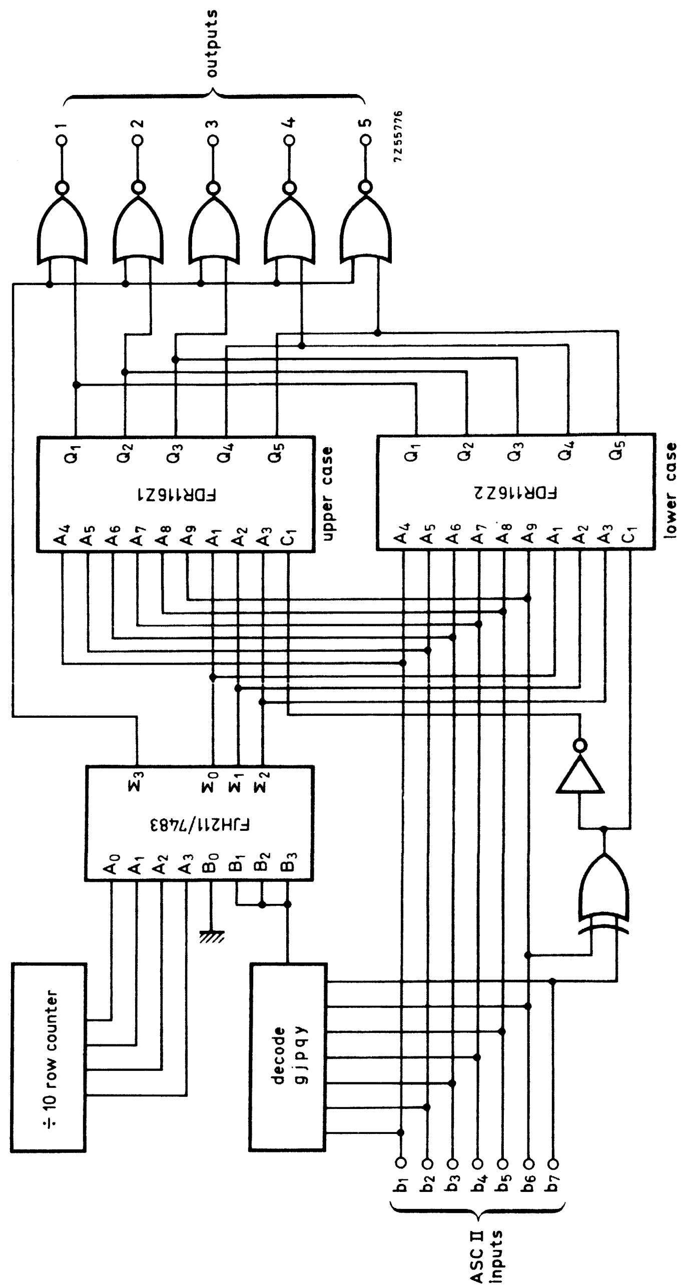
APPLICATION INFORMATION

To use the FDR116Z2 as a character generator, the ASCII code of the character to be displayed should be applied to the address inputs A_4 to A_9 with the following correspondence:

ASCII bit	address input
b_1	A_4
b_2	A_5
b_3	A_6
b_4	A_7
b_5	A_8
b_6	A_9

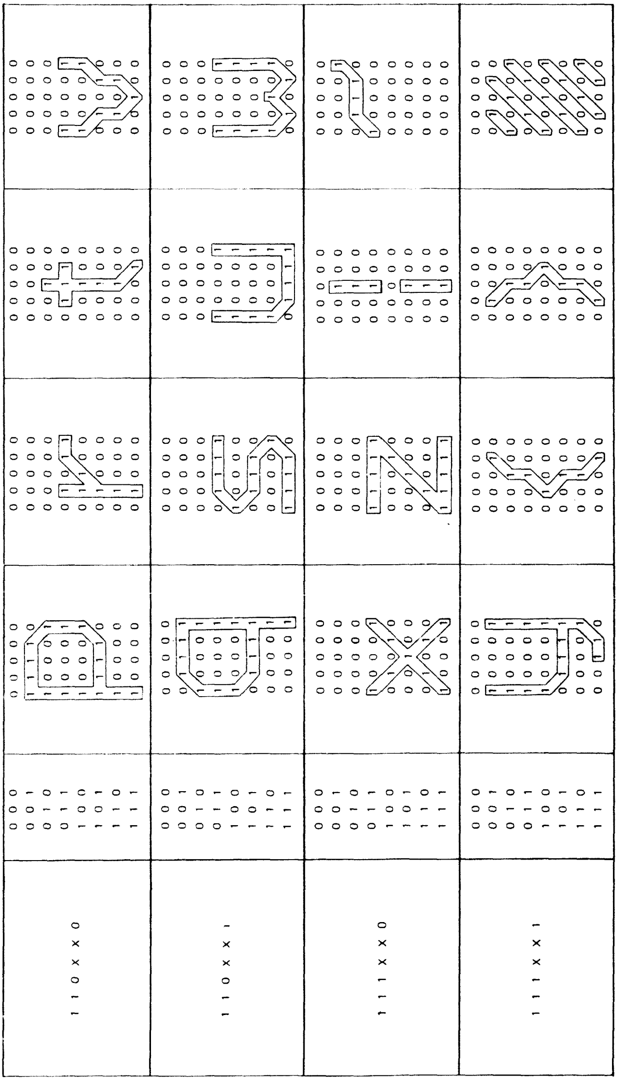
For row selection a three bit binary number should be applied to address inputs A_1 to A_3 (A_1 being the least significant bit).
On page 5 a 128 character ASCII character generator is given.
The diagram incorporates a "descender" circuit, with which the lower case g, j, p, q and y can be lowered two rows.
For this purpose an adder circuit is inserted between the row counter and the READ ONLY MEMORIES.
When a lower case g, j, p, q or y is detected a binary 2 is substracted from the row number (actually the binary number 14 is added), which causes the character to be displayed two rows lower.
The output Σ_3 of the adder is used to blank all outputs in order to avoid a repeated display of the character during rows 9 and 10 in the "normal" position, or during rows 0 and 1 in the "descended" position.

APPLICATION INFORMATION (continued)



FDR116Z2 BIT PATTERN AND FONT

ASCII CHARACTER ADDRESS INPUTS $b_6\ b_5\ b_4\ b_3\ b_2\ b_1$	LINE SELECT INPUTS	OUTPUTS			
$A_9\ A_8\ A_7\ A_6\ A_5\ A_4$	$A_3\ A_2\ A_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$
x x		00	01	10	11
1 0 0 x x 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0	0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 1 1 1 1	0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 1 1 1 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0
1 0 0 x x 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 1 0 1 1 1 1 1 0 0 0 1 0 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 1 1 1 1 1 0 0 0 0 0 1 1 1 0	0 0 0 0 0 0 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 1 1 1 1 0 0 0 0 1 0 0 1 1 0
1 0 1 x x 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1	0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0 0	0 0 0 0 0 0 1 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 1 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1
1 0 1 x x 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 1 1 0	0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 1 0 1 0 1 0 0 1 1 0 0 0 1 0 1 0 0 1 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 0 1 0 1 0 1 0 1 1 0 1 0 1 1 0 1 0 1 1 0 1 0 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 1 1 1 0



NOTE: 1 = LOW; 0 = HIGH

FDR116Z2 BIT PATTERN AND FONT (continued)

ASCII CHARACTER ADDRESS INPUTS $b_6\ b_5\ b_4\ b_3\ b_2\ b_1$	LINE SELECT INPUTS	OUTPUTS			
$A_9\ A_8\ A_7\ A_6\ A_5\ A_4$	$A_3\ A_2\ A_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$
x x →		**00**	**01**	**10**	**11**
0 0 0 x x 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 (NUL)*	0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 1 1 1 1 1 (STX)*	0 0 0 0 0 1 0 0 0 0 1 0 1 0 0 0 1 1 0 0 0 0 1 0 0 0 0 1 1 0 0 0 1 0 1 0 0 0 0 1 (EOT)*	0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0 0 0 1 0 1 0 1 0 0 1 0 1 0 0 0 1 0 0 0 (ACK)*
0 0 0 x x 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 (SOH)*	0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 1 1 1 1 1 (ETX)*	0 0 0 0 0 1 1 1 1 1 1 0 0 0 1 1 1 0 1 1 1 0 1 0 1 1 1 0 1 1 1 0 0 0 1 1 1 1 1 1 (ENQ)*	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 (BEL)*
0 0 1 x x 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 1 1 1 0 0 1 1 0 0 0 1 0 1 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 1 (BS)*	0 0 0 0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 (LF)*	0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 1 0 1 0 1 0 1 1 1 0 1 0 1 0 1 0 1 1 1 0 0 0 1 0 0 (FF)*	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 1 0 1 1 1 0 1 0 1 1 1 0 1 1 1 0 0 0 1 0 1 1 1 0 (SO)*
0 0 1 x x 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 1 1 0 0 0 0 0 1 0 0 0 0 0 1 0 1 1 1 1 1 0 0 0 1 0 0 0 1 0 0 1 1 0 0 0 (HT)*	0 0 0 0 0 1 0 1 0 1 1 0 1 0 1 1 0 1 0 1 1 0 1 0 1 0 1 1 1 0 0 1 1 1 0 0 0 1 0 0 (VT)*	0 0 0 0 0 0 0 0 1 1 0 0 1 0 0 0 1 0 0 0 1 1 1 1 1 0 1 0 0 0 0 0 1 0 0 0 0 0 1 1 (CR)*	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 0 1 0 1 1 0 0 0 1 1 0 0 0 1 0 1 1 1 0 (SI)*

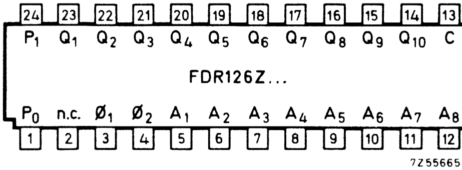
0 1 0 x x 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 (DLE)*	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 0 1 1 1 1 0 1 0 1 1 0 1 0 1 0 1 1 1 0 (DC2)*	0 0 0 0 0 0 1 1 1 0 1 0 1 0 1 1 0 1 0 1 1 1 1 0 1 1 0 0 0 1 1 0 0 0 1 0 1 1 1 0 (DC4)*	0 0 0 0 0 0 1 1 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 1 1 0 1 1 (SYN)*
0 1 0 x x 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 0 1 1 1 0 1 0 1 0 1 1 0 1 0 1 1 0 1 1 1 1 0 0 0 1 1 0 0 0 1 0 1 1 1 0 (DC1)*	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 0 1 1 0 1 0 1 1 0 1 0 1 0 1 1 1 0 (DC3)*	0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0 0 1 1 1 1 0 1 0 0 1 0 1 0 0 0 1 0 0 0 (NAK)*	0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 1 1 1 1 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 (ETB)*
0 1 1 x x 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 1 1 1 1 1 1 0 0 0 1 0 1 0 1 0 0 0 1 0 0 0 1 0 1 0 1 0 0 0 1 1 1 1 1 1 (CAN)*	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 (SUB)*	0 0 0 0 0 1 1 1 1 1 1 0 1 0 1 1 0 1 0 1 1 1 1 0 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 (FS)*	0 0 0 0 0 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 1 1 1 1 0 1 0 1 1 0 1 0 1 1 1 1 1 1 (RS)*
0 1 1 x x 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 1 1 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 (EM)*	0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 0 1 1 1 0 (ESC)*	0 0 0 0 0 1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 1 1 0 1 1 0 1 0 1 1 0 1 0 1 1 1 1 1 1 (GS)*	0 0 0 0 0 1 1 1 1 1 1 0 1 0 1 1 0 1 0 1 1 0 1 1 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 1 (US)*

* The letters in parenthesis identify the control code corresponding to the appropriate 35 Bit pictorial representation. These representations were obtained from the USASI x 3.2 Code Practice Manual.

NOTE: 1 = LOW; 0 = HIGH

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

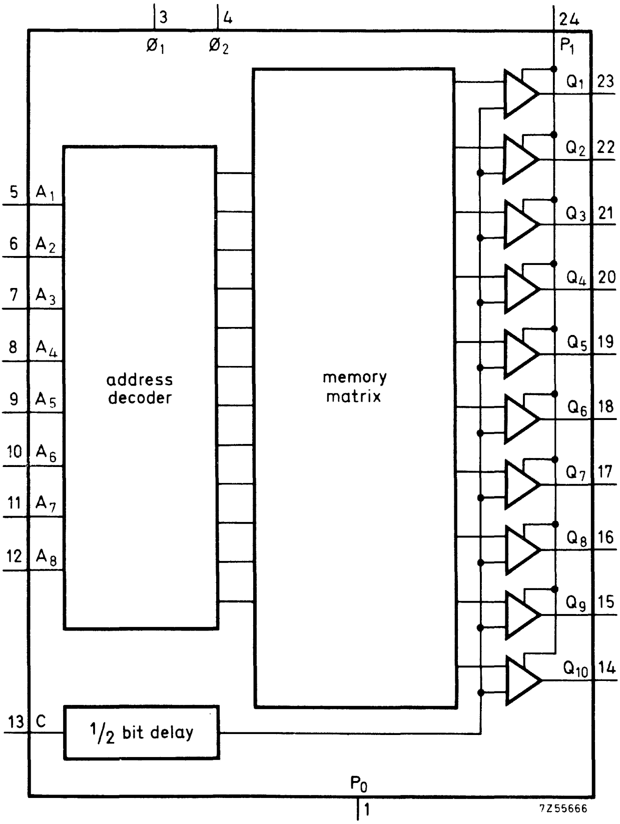
READ ONLY MEMORY, 256 WORD, 10 BITS PER WORD



P_0 and metal package bottom are connected.

QUICK REFERENCE DATA				
Read access time	t_{AR}	max.	1	µs
Clock rate	f_{ϕ}	0.1 to	1	MHz
Power dissipation at f_{ϕ} = 1 MHz	P_{av}	typ.	100	mw
D.C. noise margin	M_H, M_L	>	1.0	V
Operating ambient temperature	T_{amb}	−55 to	+85	°C

PACKAGE OUTLINE 24 lead metal ceramic dual in-line (See General Section).


3
4
24
Ø1
Ø2
P1
address
decoder
memory
matrix
5 A1
6 A2
7 A3
8 A4
9 A5
10 A6
11 A7
12 A8
13 C
1/2 bit delay
Q1 23
Q2 22
Q3 21
Q4 20
Q5 19
Q6 18
Q7 17
Q8 16
Q9 15
Q10 14
P0
1
7Z55666

GENERAL DESCRIPTION

The FDR126Z is a monolithic 2560 bit read only memory. When ordering an FDR126Z the customer must send a bit pattern matrix (see example on pages 12, 14 to 17) with the desired content. For performance evaluation, we can supply specimens of FDR126Z1, which is identical to the FDR126Z but contains a bit pattern of our own. The FDR126Z requires a two phase clock; the outputs remain steady as long as the address remains unchanged.
The memory matrix is programmed with the aid of a mask pattern during manufacture. The only d.c. supply is the output buffer supply, which is variable and can be biased to drive bipolar output loads direct.
The FDR126Z1 is a pre-programmed version of the FDR126Z READ-ONLY memory. It is intended to convert from ASCII to SELECTRIC line code and vice versa.
When 7-bit address of either code is applied to the inputs of the ROM, the corresponding 7-bits of the other code will appear at the outputs.
The three remaining outputs are used for parity and control code indications.
The electrical characteristics of the FDR126Z1 are equal to those of the FDR126Z.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_1	$-I_{P1}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125	°C/W

Note
All terminals are protected against over-voltage caused by static charges.

CHARACTERISTICS at T_{amb} = −55 to +85 °C

ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.01	–	1.0	MHz	
Clock pulse width	$t_{\phi 1L}$	0.60	–	5.0	μs	see timing diagram for parameter definitions
	$t_{\phi 2L}$	0.25	–	5.0	μs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10	μs	
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10	μs	
Clock delay time	$t_{\phi 1 \phi 2}$	0	–	45	μs	
Clock delay time	$t_{\phi 2 \phi 1}$	0	–	45	μs	
Clock input voltage level						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Address input and output inhibit input logic levels:						
HIGH	V_{AH}, V_{CH}	−2	0	+0.3	V	
LOW	V_{AL}, V_{CL}	−28	−12	−9	V	

CHARACTERISTICS (continued)

Test conditions: V_{P1} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 30 pF in parallel with 150 kΩ to P_0.

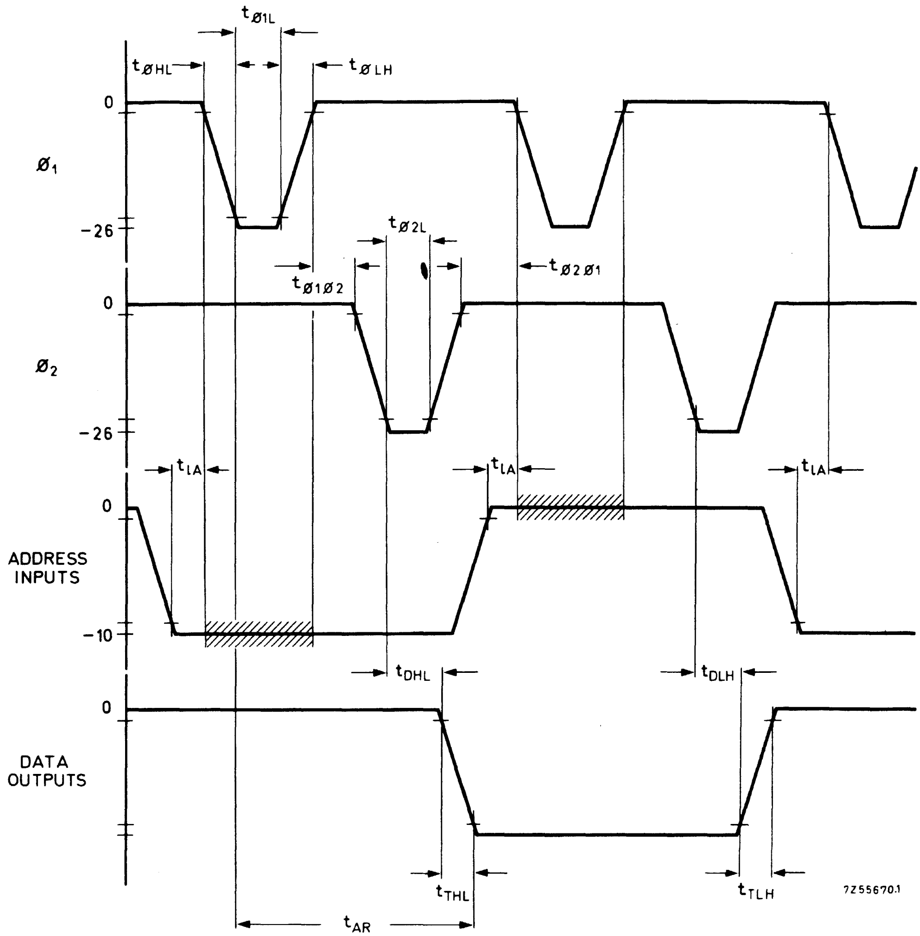
ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Read access time	t_{AR}	-	0.75	1	μs	
Output levels:						
HIGH	V_{QH}	-1	-	0	V	
LOW	V_{QL}	-14	-	-10	V	
Address input capacitance	C_A	-	3.6	5.0	pF	bias: V_A = 0 V; f_ϕ = 1 MHz
Output inhibit input capacitance	C_C	-	3.2	4.0	pF	bias: $V_C = V_\phi$ = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi1}$	-	19	30	pF	bias: $V_C = V_\phi$ = 0 V; f_ϕ = 1 MHz
	$C_{\phi2}$	-	20	30	pF	bias: $V_C = V_\phi$ = 0 V; f_ϕ = 1 MHz
	$C_{\phi1}$	-	11	20	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
	$C_{\phi2}$	-	12	20	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Leakage currents:						
Address input and output inhibit input currents	$-I_{AL}$, $-I_{CL}$	-	-	1	μA	$V_A = V_C$ = −15 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	-	-	100	μA	V_ϕ = −28 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	-	400	-	Ω	
LOW	R_{QL}	-	300	-	Ω	V_{P1} = −5 V
Clock power dissipation (see note 1) ($\phi_1 + \phi_2$)	P_ϕ	-	36	-	mW	f_ϕ = 1 MHz
Supply current (see note 2)	$-I_{P1}$	-	5.0	-	mA	V_{P1} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	-	100	-	ns	
rise time	t_{TLH}	-	100	-	ns	
Delay times: fall time	t_{DHL}	-	20	-	ns	
rise time	t_{DLH}	-	20	-	ns	
D.C. noise margin	M_L, M_H	1	-	-	V	

Note 1: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 2: I_{P1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Address and output inhibit timing requirements:

1. Address and output inhibit signals are clocked into the memory during ϕ_1, and must remain present throughout ϕ_1. Address and output inhibit lead time ($t_{\ell A}$) must be ≥ 0, during the shaded interval.
2. The output signals remain steady for as many clock cycles as the address and output inhibit signals remain unchanged.

Note:
The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

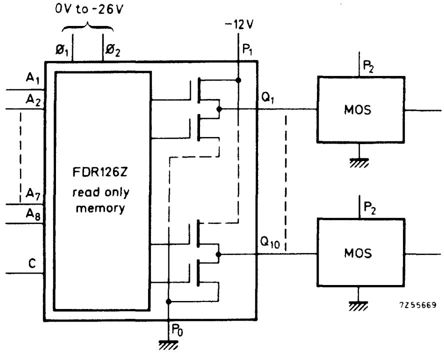
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V.
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Fall delay time: t_{DHL}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Output inhibit time: t_{CL}
   The minimum time that the output inhibit signal must be present during ϕ_2 in order to inhibit the output, defined at −2 V.
10. Read access time: t_{AR}
    The time between the 90% point on the leading edge of the clock pulse ϕ_1 and the time at which the output is present.

OUTPUT BUFFER DESCRIPTION

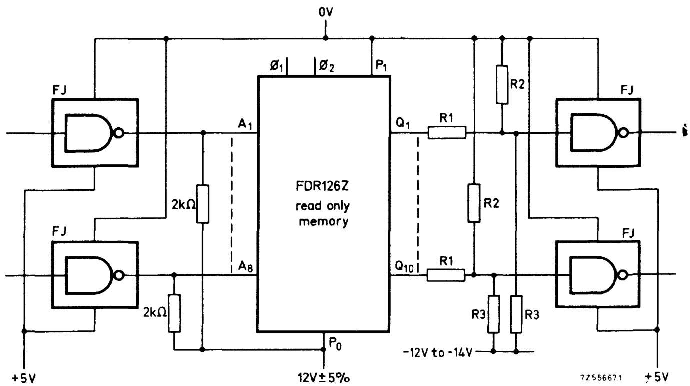
The only d.c. supply required is V_{P1}, the push-pull output buffer supply. V_{P1} may be varied between 0 and −28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A

2. Biasing circuit B is used when driving TTL loads direct from each output buffer. This circuit allows also to drive MOS circuits direct from TTL. For this purpose special TTL gates are available (FJH301, FJH311 and FJH321), with a guaranteed minimum output breakdown voltage of 15 V.

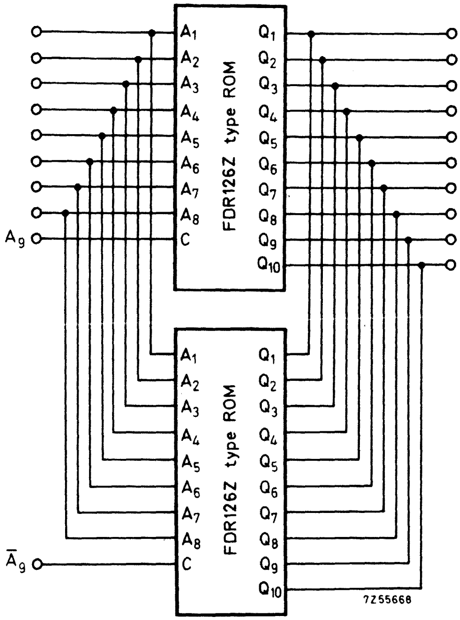


R1 = 820 Ω
R2 = 820 Ω
R3 = 12 kΩ
All resistors: ± 5%

Biasing circuit B

WIRED-OR APPLICATIONS

Use of wired-or output capability:
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-or with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. This output inhibit wired-or capability makes it possible to use the FDR126Z type ROM in many different applications, such as those shown here. Note that the terminals A9 and $\overline{A9}$ although shown as address inputs, must actually be output inhibit signals synchronous with the address.



PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 12. Four forms are needed for 256 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched card are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customers's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made and the unique type number suffix is assigned.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS
   a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left hand bit is bit 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.
   b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
   c) Bits 7, 8 and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1])
   Memories of 256 words need 4 pages, of specifications.
   d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form except where, as with 256 word memories, column 9 is unused and is, therefore, left blank.

---

[1]) See example on page 12.

2. CONTENTS (DATA OUTPUTS)
   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 10 using only ones (1 = LOW) and zeros (0 = HIGH), except where a column is unused and is, therefore, left blank.

3. AUTHORIZED SIGNATURE
   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

IIIIIII

PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern FDR 126 ...

page of

AUTHORIZED SIGNATURE

CUSTOMER NAME:

DATE

ADDRESS INPUTS 9 8 7 6 5 4 3 2 1 (1 2 3 . . 4 5 6 7)	CONTENTS 00 OUTPUTS 10 9 8 7 6 5 4 3 2 1 (8–17)	CONTENTS 01 OUTPUTS 10 9 8 7 6 5 4 3 2 1 (18–27)	CONTENTS 10 OUTPUTS 10 9 8 7 6 5 4 3 2 1 (28–37)	CONTENTS 11 OUTPUTS 10 9 8 7 6 5 4 3 2 1 (38–47)
XX0000				
XX0001				
XX0010				
XX0011				
XX0100				
XX0101				
XX0110				
XX0111				
XX1000				
XX1001				
XX1010				
XX1011				
XX1100				
XX1101				
XX1110				
XX1111				

Note: 1 = LOW; 0 = HIGH

GENERAL DESCRIPTION of FDR126Z1

The FDR126Z1 is a version of the FDR126Z pre-programmed to convert from ASCII to SELECTRIC line code and vice versa.
When any 7-bit address of either code is presented to the input the FDR126Z1 will deliver the corresponding word at its output.
The direction of conversion is selected with the eighth address input.
The correspondence between code bits and inputs and outputs is shown in the table below.

address input	ASCII bit	SELECTRIC bit	output
A_1	b_1	1	Q_1
A_2	b_2	2	Q_2
A_3	b_3	4	Q_3
A_4	b_4	8	Q_4
A_5	b_5	A	Q_5
A_6	b_6	B	Q_6
A_7	b_7	S	Q_7

A_8 = LOW: conversion from SELECTRIC line code to ASCII.

A_8 = HIGH: conversion from ASCII to SELECTRIC line code.

Output Q_8 adds an odd parity bit to the 7-bit output code on Q_1 to Q_7 (see note).

Output Q_9 LOW indicates odd parity at the input.

Comparison of the Q_9 output with the parity bit added to the input word indicates whether or not the input code is correct.

If Q_{10} is LOW, the word on outputs Q_1 to Q_7 is a line control code.

Note:
1 = LOW; 0 = HIGH

ASCII CODE

b7 / b6 / b5 →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 b3 b2 b1 ↓	row ↓ / column →	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL / IL1	DLE / PRE2	SPACE / SPACE1	0 / 0	@ / @	P / P	\ / |	p / p
0 0 0 1	1	SOH / b	DC1 / RS2	! / !	| / |	A / A	Q / Q	a / a	q / q
0 0 1 0	2	STX / 9	DC2 / PN1	" / "	2 / 2	B / B	R / R	b / b	r / r
0 0 1 1	3	ETX / EOB1	DC3 / RS1	# / #	3 / 3	C / C	S / S	c / c	s / s
0 1 0 0	4	EOT / EOT1	DC4 / PF1	$ / $	4 / 4	D / D	T / T	d / d	t / t
0 1 0 1	5	ENQ / UC2	NAK / !	% / %	5 / 5	E / E	U / U	e / e	u / u
0 1 1 0	6	ACK / –	SYN / IL2	& / &	6 / 6	F / F	V / V	f / f	v / v
0 1 1 1	7	BEL / LC1	ETB / EOB2	/ / |	7 / 7	G / G	W / W	g / g	w / w

Note: 1 = LOW; 0 = HIGH

ASCII CODE (continued)

b7 → b6 → b5 →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 b3 b2 b1 ↓	column → / row ↓	0	1	2	3	4	5	6	7
1 0 0 0	8	BS / BS1	CAN / !	(/ (	8 / 8	H / H	X / X	h / h	x / x
1 0 0 1	9	HT / HT1	EM / RES1	) /)	9 / 9	I / I	Y / Y	i / i	y / y
1 0 1 0	10	LF / LF1	SUB / BY1	* / *	: / :	J / J	Z / Z	j / j	z / z
1 0 1 1	11	VT / ②	ESC / PRE1	+ / +	; / ;	K / K	[/ ±	k / k	[/ ±
1 1 0 0	12	FF / ⑤	FS / BY2	, / ,	< / o	L / L	\ / ±	! / !	: / ±
1 1 0 1	13	CR / NL1	GS / RES2	– / –	= / =	M / M	] / ±	m / m	] / ±
1 1 1 0	14	SO / UC1	RS / RES2	. / .	> / ¢	N / N	⌢ / ±	n / n	~ / ±
1 1 1 1	15	SI / LC2	US / BY2	/ / /	? / ?	O / O	– / –	o / o	DEL / DEL1

Note: 1 = LOW; 0 = HIGH

SELECTRIC LINE CODE TO ASCII CODE CORRESPONDENCE

S → B → A →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
8 4 2 1 ↓	row ↓ / column →	0	1	2	3	4	5	6	7
0 0 0 0	0	SPACE1 / SPACE	t / t	! / !	j / j	SPACE2 / SPACE	T / T	o / <	J / J
0 0 0 1	1	1 / 1	x / x	m / m	g / g	± /]	X / X	M / M	G / G
0 0 1 0	2	2 / 2	n / n	. / .	= / =	@ / @	N / N	. / .	+ / +
0 0 1 1	3	3 / 3	u / u	v / v	f / f	# / #	U / U	V / V	F / F
0 1 0 0	4	5 / 5	e / e	| / /	p / p	% / %	E / E	" / "	P / P
0 1 0 1	5	7 / 7	d / d	r / r	; / ;	& / &	D / D	R / R	: / :
0 1 1 0	6	6 / 6	k / k	i / i	q / q	¢ / >	K / K	I / I	Q / Q
0 1 1 1	7	8 / 8	c / c	a / a	, / ,	* / *	C / C	A / A	, / ,

Note: 1 = LOW; 0 = HIGH

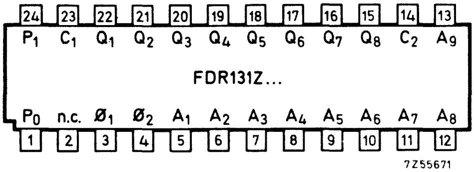
SELECTRIC LINE CODE TO ASCII CODE CORRESPONDENCE (continued)

S B A →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
8 4 2 1 ↓	row ↓ / column →	0	1	2	3	4	5	6	7
1 0 0 0	8	4 / 4	| / |	o / o	/ / /	$ / $	L / L	O / O	? / ?
1 0 0 1	9	0 / 0	h / h	s / s	y / y	) /)	H / H	S / S	Y / Y
1 0 1 0	10	z / z	① / RS	② / VT	③ / RS	Z / Z	④ / RS	⑤ / FF	⑥ / RS
1 0 1 1	11	9 / 9	b / b	w / w	– / –	(/ (	B / B	W / W	– / –
1 1 0 0	12	PN1 / DC2	BY1 / SUB	RES1 / EM	PF1 / DC4	PN2 / DC2	BY2 / FS	RES2 / GS	PF2 / DC4
1 1 0 1	13	RS1 / DC3	LF1 / LF	NL1 / CR	HT1 / HT	RS2 / DC1	LF2 / LF	NL2 / CR	HT2 / HT
1 1 1 0	14	UC1 / SO	EOB1 / ETX	BS1 / BS	LC1 / BEL	UC2 / ENQ	EOB2 / ETB	BS2 / BS	LC2 / SI
1 1 1 1	15	EOT1 / EOT	PRE1 / ESC	IL1 / NUL	DEL1 / DEL	EOT2 / EOT	PRE2 / DLE	IL2 / NUL	DEL2 / NUL

Note: 1 = LOW; 0 = HIGH

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

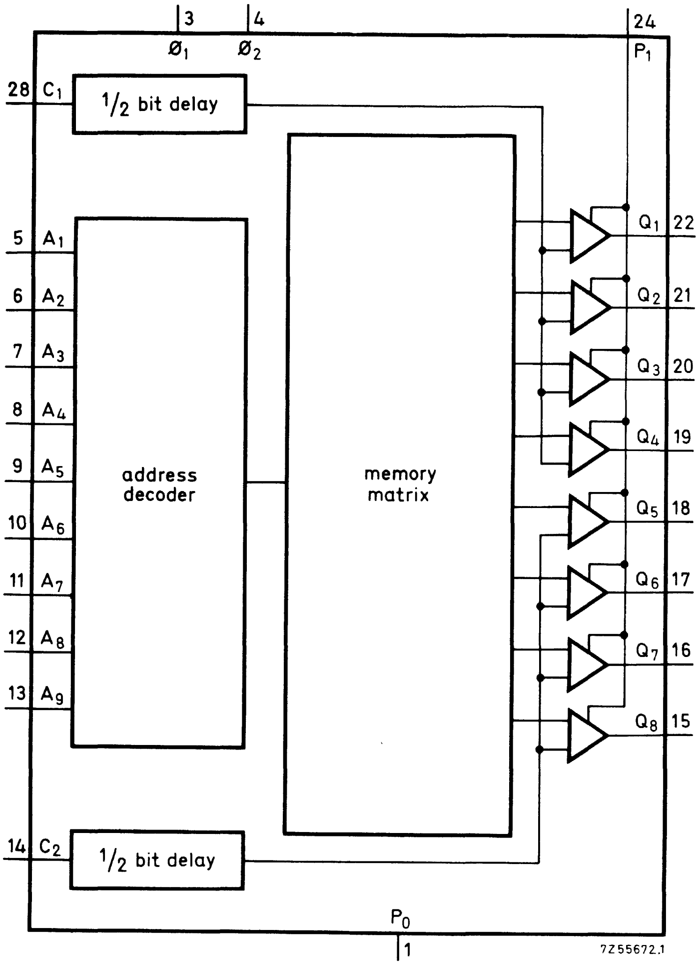
READ ONLY MEMORY, 512 WORD, 8 BITS PER WORD



P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA				
Read access time	t_{AR}	max.	1.5	μs
Clock rate	f_{ϕ}	max.	0.66	MHz
Power dissipation (MOS load)	P_{tot}	typ.	100	mW
D.C. noise margin	M_H, M_L	>	1.0	V
Operating ambient temperature	T_{amb}		0 to 70	°C

PACKAGE OUTLINE 24 lead metal ceramic dual in-line (See General Section).


3
4
Ø1
Ø2
24
P1
28
C1
1/2 bit delay
5
A1
6
A2
7
A3
8
A4
9
A5
10
A6
11
A7
12
A8
13
A9
address decoder
memory matrix
Q1 22
Q2 21
Q3 20
Q4 19
Q5 18
Q6 17
Q7 16
Q8 15
14
C2
1/2 bit delay
P0
1
7Z55672.1

GENERAL DESCRIPTION

The FDR131Z is a monolithic 4096-bit READ-only memory (ROM) with a capacity of 512 words, 8 bits per word. With two output-inhibit control lines C_1 and C_2 it can also operate as a 1024-word, 4 bits per word memory. The memory matrix is given the desired content by means of a special mask. When ordering, customers have to complete a set of forms specifying the bit pattern to be associated with each address. The output-inhibit control make it possible to use several FDR131Z memories in wired-OR configuration.
The only d.c. supply is the output buffer supply (P_1), which may be adapted to interface direct with either MOS or bipolar DTL/TTL. All terminals of the FD circuits are effectively protected against over voltage caused by static charge.
A pre-programmed specimen of the FDR131Z is the FDR131Z1 given on page 14.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_1	$-I_{P1}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	°C/W

CHARACTERISTICS at T_{amb} = 0 to +70 °C

ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.1	-	0.66	MHz	(see note)
Clock pulse width	$t_{\phi 1L}$	0.90	-	2.0	μs	see timing diagram for parameter definitions
	$t_{\phi 2L}$	0.35	-	2.0	μs	
Clock pulse rise time (ϕ_1, ϕ_2)	$t_{\phi LH}$	-	-	1.0	μs	See note
Clock pulse fall time	$t_{\phi 1HL}$	0.165	-	1.0	μs	See note
	$t_{\phi 2HL}$	-	-	1.0	μs	See note
Clock delay time	$t_{\phi 1 \phi 2}$	0	-	4.5	μs	
Clock delay time	$t_{\phi 2 \phi 1}$	0	-	4.5	μs	
Clock input voltage level						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Address input and output inhibit input logic levels:						
HIGH	V_{AH}, V_{CH}	−2	0	+0.3	V	
LOW	V_{AL}, V_{CL}	−14	−12	−9	V	

Note:
At frequencies higher than 191 kHz the maximum clock pulse rise and fall times will be determined by the minimum ϕ_1 and ϕ_2 pulse width.

CHARACTERISTICS

Test conditions: V_{P1} = −12 V to −14 V; T_{amb} = 0 to +70 °C; P_0 = grounded; standard load: 30 pF in parallel with 150 kΩ to P_0.

ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Read access time	t_{AR}	-	1.2	1.5	μs	see note 1
Output levels:						
HIGH	V_{QH}	−1	-	0	V	
LOW	V_{QL}	−14	-	−10	V	
Address input and output inhibit input capacitances	C_A, C_C	-	3.2	4.0	pF	bias: $V_A = V_C$ = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$	-	18	22	pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	-	16	20	pF	
	$C_{\phi 1}$	-	11	14	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	-	9.5	12	pF	
Leakage currents:						
Address input and output inhibit input currents	$-I_{AL}$, $-I_{CL}$	-	-	1	μA	$V_A = V_C$ = −15 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	-	-	100	μA	V_ϕ = −28 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	-	500	-	Ω	
LOW	R_{QL}	-	350	-	Ω	V_{P1} = −5 V
Clock power dissipation (see note 2) ($\phi_1 + \phi_2$)	P_ϕ	-	36	-	mW	f_ϕ = 1 MHz
Supply current (see note 3)	$-I_{P1}$	-	4.0	-	mA	V_{P1} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times: fall time	t_{THL}	-	200	-	ns	
rise time	t_{TLH}	-	200	-	ns	
Delay times: fall time	t_{DHL}	-	20	-	ns	
rise time	t_{DLH}	-	20	-	ns	
D.C. noise margin	M_L, M_H	1	-	-	V	

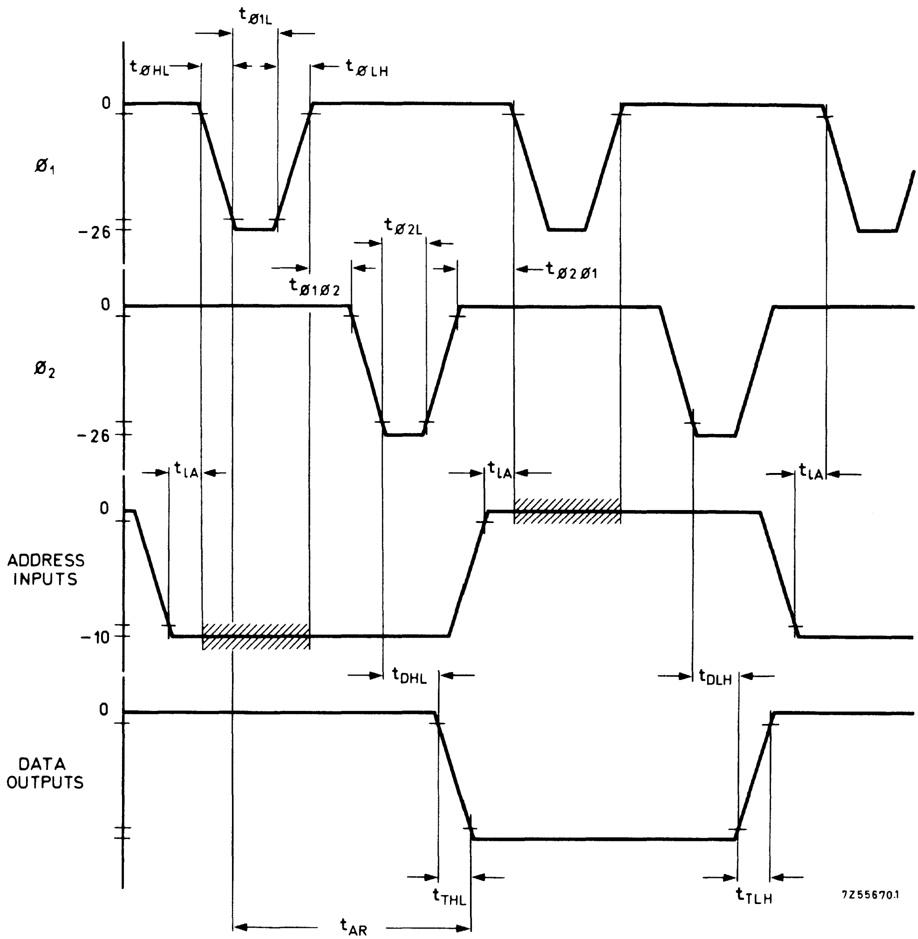
Note 1: Assuming the fall time of ϕ_1 and rise time of ϕ_2 is less than 40 ns.

Note 2: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 3: I_{P1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Address and output inhibit requirements:

1. Address and output inhibit signals are clocked into the memory during ϕ_1, and must remain present during the shaded interval. Address lead time ($t_{\ell A}$) must be ≥ 0.
2. The output signals remain steady when the address and output inhibit signals remain unchanged.

Note:

The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

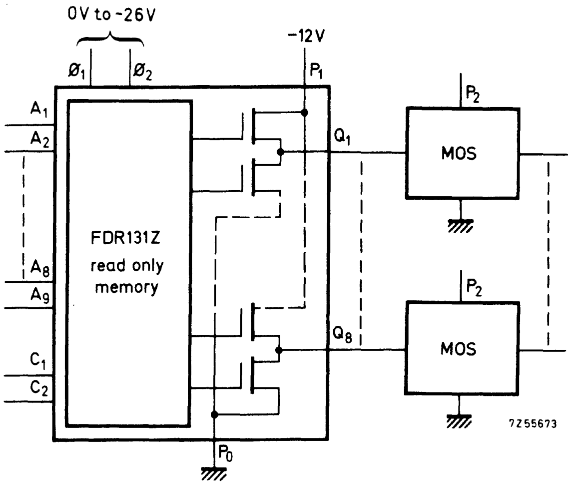
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Fall delay time: t_{DHL}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output start to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Read acces time: t_{AR}
   The time between the 90% point on the leading edge of the clock pulse ϕ_1 and the time at which the output is present, defined at 90%.

OUTPUT BUFFER DESCRIPTION

The only d.c. supply required is V_{P1}, the push-pull output buffer supply. V_{P1} may be varied between 0 and −28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

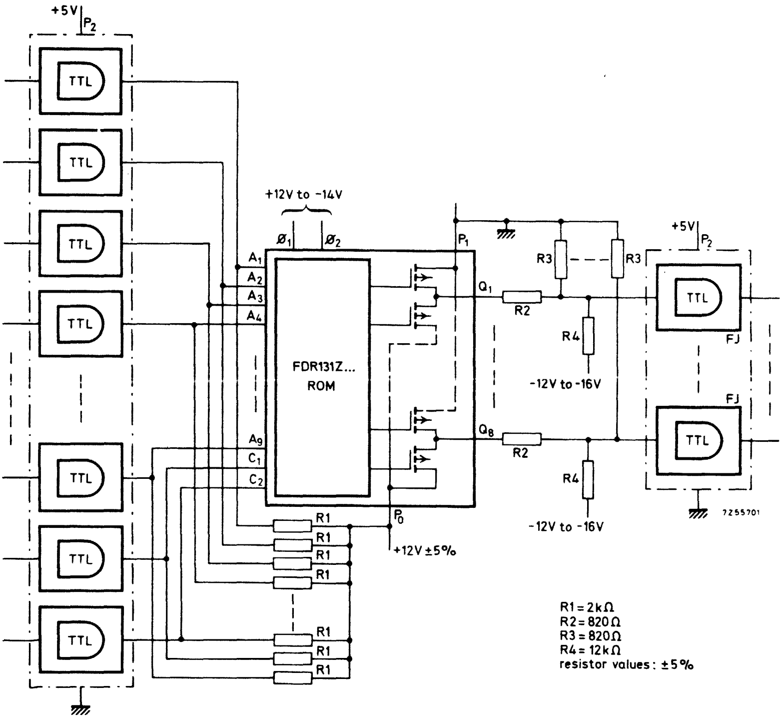
1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A

OUTPUT BUFFER DESCRIPTION (continued)

2. Biasing circuit B is used to interface direct with TTL on both the inputs and outputs of the READ-only memory. No active interface components are required. The TTL circuits on the inputs of the ROM must be able to sustain at least +12 V at their outputs.
   The quadruple NAND gate FJH301 and the sextuple inverter FJH321 are especially manufactured with a guaranteed breakdown voltage of 15 V for this purpose.

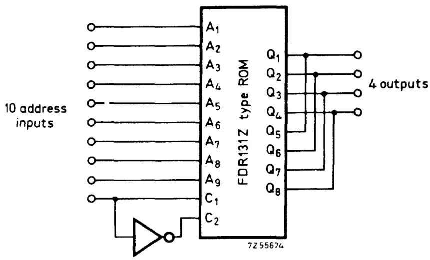


WIRED-OR APPLICATIONS

Use of wired-or output capability:
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-or with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. C_1 controls output buffers 1 to 4, and C_2 controls output buffers 5 to 8. This output inhibit wired-or capability makes it possible to use the FDR131Z type ROM in many different applications, such as those shown here.

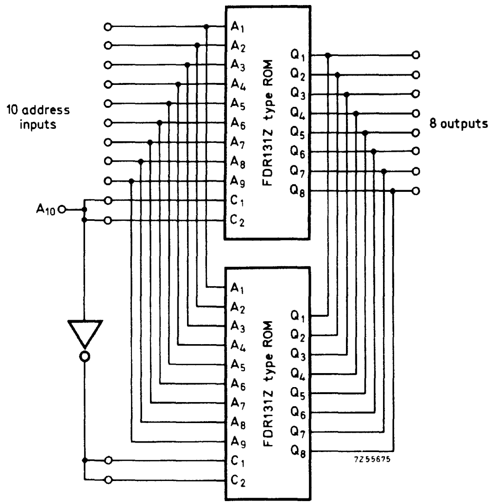
1024 words

4-bits per word



1024 words

8-bits per word



PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 13. Eight forms are needed for 512 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched cards are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customer's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made and the unique type number suffix is assigned.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid-out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS
   a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.
   b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
   c) Bit 7, 8, and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1]
   Memories of 256 words need 4 pages, of specifications.
   d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form except where, a column is unused and is, therefore, left blank.

[1]) See example on page 13

2. CONTENTS (DATA OUTPUTS)
   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 10 using only ones (1 = LOW) and zeros (0 = HIGH), except where a column is unused and is, therefore, left blank.

3. AUTHORIZED SIGNATURE
   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern FDR 131...

page of

AUTHORIZED SIGNATURE

CUSTOMER NAME:

DATE

CONTENTS

ADDRESS INPUTS									00 OUTPUTS										01 OUTPUTS										10 OUTPUTS										11 OUTPUTS									
9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1
1	2	3	-	-	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
			X	X	0	0	0	0																																							
			X	X	0	0	0	1																																							
			X	X	0	0	1	0																																							
			X	X	0	0	1	1																																							
			X	X	0	1	0	0																																							
			X	X	0	1	0	1																																							
			X	X	0	1	1	0																																							
			X	X	0	1	1	1																																							
			X	X	1	0	0	0																																							
			X	X	1	0	0	1																																							
			X	X	1	0	1	0																																							
			X	X	1	0	1	1																																							
			X	X	1	1	0	0																																							
			X	X	1	1	0	1																																							
			X	X	1	1	1	0																																							
			X	X	1	1	1	1																																							

Note: 1 = LOW; 0 = HIGH

GENERAL DESCRIPTION of FDR131Z 1

The FDR131Z1 is a version of the FDR131Z pre-programmed to convert frpm ASCII to EBCDIC and vice versa.
When the standard 7-bit ASCII code plus parity is presented to address inputs A_1 to A_8, the FDR131Z1 will deliver the corresponding 8-bit EBCDIC code at its outputs when the A_9 input is HIGH. Conversely, when the standard 8-bit EBCDIC code is presented to inputs A_1 to A_8, the corresponding ASCII code plus parity will be delivered at the outputs when A_9 is LOW. The code conversion circuits from ASCII to EBCDIC are provided in duplicate to accomodate either odd or even parity. The correspondence between code bits and inputs and outputs is shown in the tables below and on the following pages.

Conversion from ASCII to EBCDIC

ASCII-bits	ROM inputs [1]	ROM outputs	EBCDIC-bits
b_1 (least significant bit)	A_1	Q_1	7 (least significant bit)
b_2	A_2	Q_2	6
b_3	A_3	Q_3	5
b_4	A_4	Q_4	4
b_5	A_5	Q_5	3
b_6	A_6	Q_6	2
b_7 (most significant bit)	A_7	Q_7	1
b_8 (odd or even paratity)	A_8	Q_8	0 (most significant bit)

Correspondence of ASCII(A) to EBCDIC(E) code

To find the 7-bit ASCII code for a particular symbol, (see table on page 15) write down the binary coded decimal number belonging to that symbol; e.g., the number belonging to the letter g is 103, which means that the corresponding binary digits for bits b_7 to b_1 of the ASCII code are 1100111.

[1] Condition: A9 is HIGH

Correspondence of ASCII(A) to EBCDIC(E) code (continued)

	0-15		16-31		32-47		48-63		64-79		80-95		96-111		112-127	
	A	E	A	E	A	E	A	E	A	E	A	E	A	E	A	E
0	NUL	NUL	DLE	DLE	SP	SP	0	0	@	@	P	P	`	'	p	p
1	SOH	SOH	DC1	DC1	!	!	1	1	A	A	Q	Q	a	a	q	q
2	STX	STX	DC2	DC2	"	"	2	2	B	B	R	R	b	b	r	r
3	ETX	ETX	DC3	DC3	#	#	3	3	C	C	S	S	c	c	s	s
4	EOT	EOT	DC4	DC4	$	$	4	4	D	D	T	T	d	d	t	t
5	ENQ	ENQ	NAK	NAK	%	%	5	5	E	E	U	U	e	e	u	u
6	ACK	ACK	SYN	SYN	&	&	6	6	F	F	V	V	f	f	v	v
7	BEL	BEL	ETB	EOB	'	'	7	7	G	G	W	W	g	g	w	w
8	BS	BS	CAN	CAN	(	(	8	8	H	H	X	X	h	h	x	x
9	HT	HT	EM	EM	)	)	9	9	I	I	Y	Y	i	i	y	y
10	LF	LF	SUB	SUB	*	*	:	:	J	J	Z	Z	j	j	z	z
11	VT	VT	ESC	PRE	+	+	;	;	K	K	[	(	k	k	{	(
12	FF	FF	FS	IFS	,	,	<	<	L	L	\	/	l	l	¦	|
13	CR	CR	GS	IGS	–	–	=	=	M	M	]	)	m	m	}	)
14	SO	SO	RS	IRS	.	.	>	>	N	N	⌢	¬	n	n	~	¢
15	SI	SI	US	IUS	/	/	?	?	O	O	_	_	o	o	DEL	DEL

Explanation of symbols

NUL = null
SOH = start of heading
STX = start of text
ETX = end of text
EOT = end of transmission
ENQ = enquiry
ACK = acknowledge
BEL = bell
BS = backspace
HT = horizontal tab
FF = form-feed
CR = carriage return
SO = shift out
SI = shift in

DLE = data link escape
DC1 to DC4 = device control
NAK = negative acknowledge
SYN = synchronous idle
ETB = end of transmission block
CAN = cancel
EM = end of medium
SUB = substitute
ESC = escape
FS = file separator
GS = group separator
RS = record separator
US = unit separator
DEL = delete (rub out)

The ASCII to EBCDIC characters for which there was no correspondence have been converterd as follows:

128-ASCII	256-EBCDIC
[	(
\	/
]	)
⌢	¬

128-ASCII	256-EBCDIC
`	' 1)
{	(
}	)
~	¢

1) The EBCDIC to ASCII is ' to '

Conversion from EBCDIC to ASCII

When the standard 8-bit EBCDIC code is presented to inputs A_1 to A_8, the corresponding ASCII code plus parity will be delivered at the outputs when A_9 is LOW.

EBCDIC-bits	ROM-inputs [1])	ROM-outputs	ASCII-bits
7 (least significant bit)	A_1	Q_1	b_1 (least significant bit)
6	A_2	Q_2	b_2
5	A_3	Q_3	b_3
4	A_4	Q_4	b_4
3	A_5	Q_5	b_5
2	A_6	Q_6	b_6
1	A_7	Q_7	b_7 (most significant bit)
0 (most significant bit)	A_8	Q_8	b_8 (even parity)

Correspondence of EBCDIC to ASCII code

	0-15		16-31		32-47		48-63		64-79		80-95		96-111		112-127	
	E	A	E	A	E	A	E	A	E	A	E	A	E	A	E	A
0	NUL	NUL	DLE	DLE	DS	–	–	–	SP	SP	&	&	–	–	–	–
1	SOH	SOH	DC1	DC1	SOS	–	–	–	–	–	–	–	/	/	–	–
2	STX	STX	DC2	DC2	FS	–	SYN	SYN	–	–	–	–	–	–	–	–
3	ETX	ETX	DC3	DC3	–	–	–	–	–	–	–	–	–	–	–	–
4	PF	–	RES	–	BYP	–	PN	–	–	–	–	–	–	–	–	–
5	HT	HT	NL	–	LF	LF	RS	–	–	–	–	–	–	–	–	–
6	LC	–	BS	BS	EOB	ETB	VC	–	–	–	–	–	–	–	–	–
7	DEL	DEL	IL	–	PRE	ESC	EOT	EOT	–	–	–	–	–	–	–	–
8	–	–	CAN	CAN	–	–	–	–	–	–	–	–	–	–	–	–
9	–	–	EM	EM	–	–	–	–	–	–	–	–	–	–	–	–
10	SMM	–	CC	–	SM	–	–	–	¢	–	!	!	–	–	:	:
11	VT	VT	–	–	–	–	–	–	.	.	$	$	,	,	#	#
12	FF	FF	IFS	FS	–	–	DC4	DC4	<	<	*	*	%	%	@	@
13	CR	CR	IGS	GS	ENQ	ENQ	NAK	NAK	(	(	)	)	–	–	,	'
14	SO	SO	IRS	RS	ACK	ACK	–	–	+	+	;	;	>	>	=	=
15	SI	SI	IUS	US	BEL	BEL	SUB	SUB	|	:	¬	–	?	?	"	"

[1]) Condition: A_9 = LOW

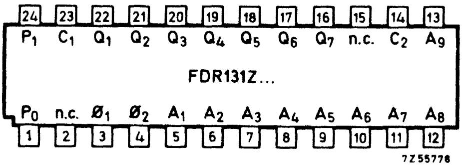
Correspondence of EBCDIC to ASCII code (continued)

To find the 8-bit EBCDIC code for a particular symbol (see table below and on page 16), write down the decimal number belonging to that symbol; e.g., the number belonging to the letter g is 135, which means the corresponding number for the bit positions 0 to 7 of the EBCDIC code is 10000111.

128-143		144-159		160-175		176-191		192-207		208-223		224-239		240-255	
E	A	E	A	E	A	E	A	E	A	E	A	E	A	E	A
–	–	–	–	–	–	–	–	–	–	–	–	–	–	0	0
a	a	j	j	–	–	–	–	A	A	J	J	–	–	1	1
b	b	k	k	s	s	–	–	B	B	K	K	S	S	2	2
c	c	l	l	t	t	–	–	C	C	L	L	T	T	3	3
d	d	m	m	u	u	–	–	D	D	M	M	U	U	4	4
e	e	n	n	v	v	–	–	E	E	N	N	V	V	5	5
f	f	o	o	w	w	–	–	F	F	O	O	W	W	6	6
g	g	p	p	x	x	–	–	G	G	P	P	X	X	7	7
h	h	q	q	y	y	–	–	H	H	Q	Q	Y	Y	8	8
i	i	r	r	z	z	–	–	I	I	R	R	Z	Z	9	9
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

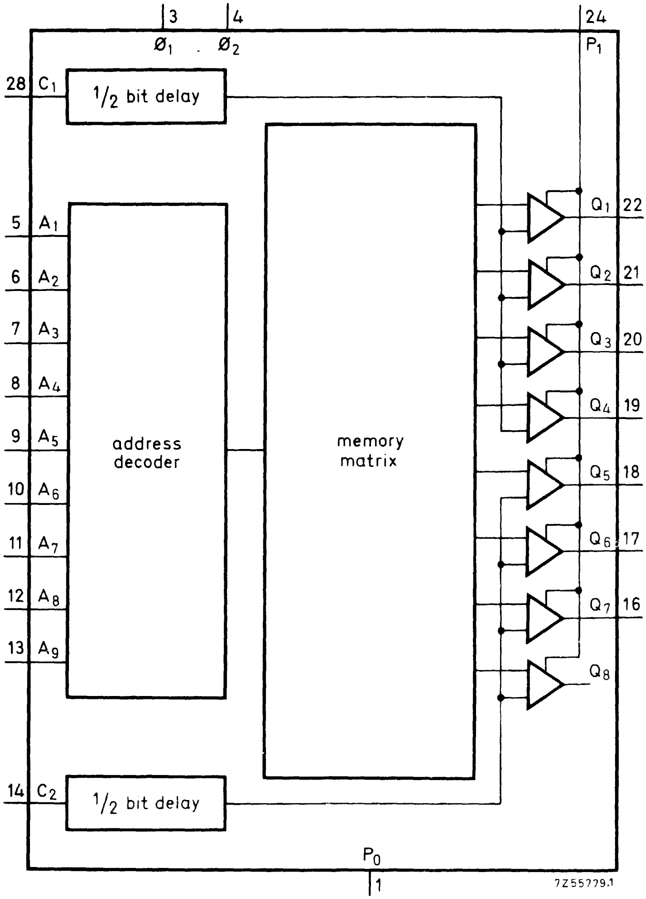
CHARACTER GENERATOR (5 × 7 DOT MATRIX; COLUMN SCAN SYSTEM)



P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA				
Read access time	t_{AR}	max.	1.5	μs
Clock rate	f_ϕ	max.	0.67	MHz
Power dissipation at f_ϕ = 0.67 MHz	P_{av}	typ.	90	mW
D.C. noise margin	M_H, M_L	>	1.0	V
Operating ambient temperature	T_{amb}	0 to	+70	°C

PACKAGE OUTLINE 24 lead metal ceramic dual in-line (See General Section).



GENERAL DESCRIPTION

The FDR131Z2 is a pre-programmed version of the FDR131Z.
It is inteded for use as alphanumeric character generator in display systems, using a 5 x 7 dot matrix, where the characters are built-up column-wise. The CHARACTER SELECT inputs (A_4 to A_9) accept a six bit ASCII code, for the COLUMN SELECT inputs (A_1 to A_3) a three bit binary number is required, which is internally decoded. Each 7-bit word appears in parallel on the 7 outputs.

RATINGS

CHARACTERISTICS

OUTPUT BUFFER DESCRIPTION

For this information see data sheets of FDR131Z

APPLICATION INFORMATION

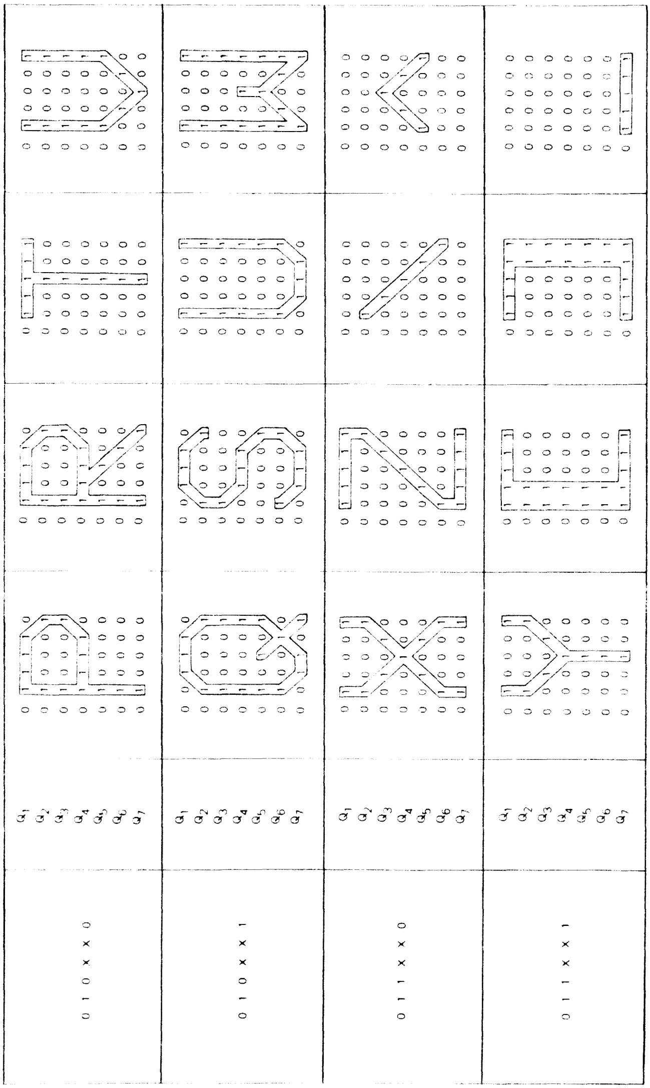
To use the FDR131Z2 as character generator the ASCII code of the desired character should be applied to the address inputs A_4 to A_9 with the following correspondence:

ASCII bit	address input
b_1	A_4
b_2	A_5
b_3	A_6
b_4	A_7
b_5	A_8
b_6 or $\overline{b_7}$	A_9

Fot column selection, a three bit binary number should be applied to the address inputs A_1 to A_3 (A_1 being the least significant bit).
The character is stored in the columns 001 to 101. Column 000 contains blanks only and can be used to a space between characters.
When a LOW signal is applied to the output inhibit inputs, all outputs become floating. This feature can be used in wired-OR applications.

FDR131Z2 BIT PATTERN AND FONT

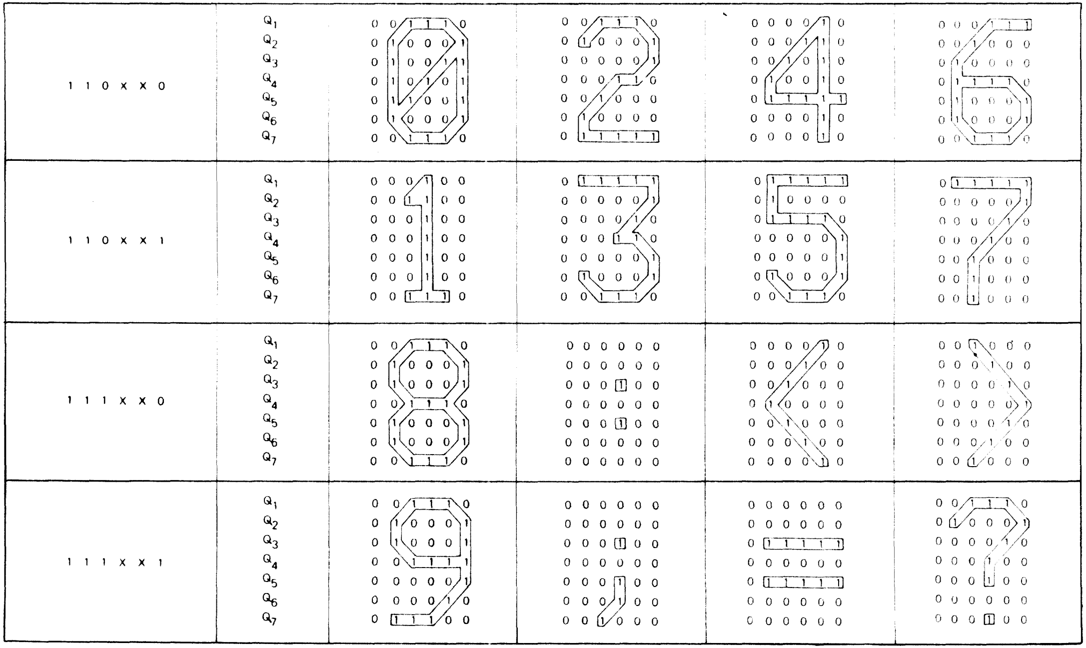
ASCII CHARACTER ADDRESS INPUTS $b_6\ b_5\ b_4\ b_3\ b_2\ b_1$	ROM OUTPUTS	COLUMN SELECT INPUTS			
		A1 0 1 0 1 0 1	A1 0 1 0 1 0 1	A1 0 1 0 1 0 1	A1 0 1 0 1 0 1
		A2 0 0 1 1 0 0	A2 0 0 1 1 0 0	A2 0 0 1 1 0 0	A2 0 0 1 1 0 0
A9 A8 A7 A6 A5 A4		A3 0 0 0 0 1 1	A3 0 0 0 0 1 1	A3 0 0 0 0 1 1	A3 0 0 0 0 1 1
x x →		00	01	10	11
0 0 0 x x 0	Q1	0 0 1 1 1 0	0 1 1 1 1 0	0 1 1 1 1 0	0 1 1 1 1 1
	Q2	0 1 0 0 0 1	0 1 0 0 0 1	0 1 0 0 0 1	0 1 0 0 0 0
	Q3	0 1 0 1 0 1	0 1 0 0 0 1	0 1 0 0 0 1	0 1 0 0 0 0
	Q4	0 1 0 1 1 1	0 1 1 1 1 0	0 1 0 0 0 1	0 1 1 1 1 0
	Q5	0 1 0 1 1 0	0 1 0 0 0 1	0 1 0 0 0 1	0 1 0 0 0 0
	Q6	0 1 0 0 0 0	0 1 0 0 0 1	0 1 0 0 0 1	0 1 0 0 0 0
	Q7	0 0 1 1 1 1	0 1 1 1 1 0	0 1 1 1 1 0	0 1 0 0 0 0
0 0 0 x x 1	Q1	0 0 0 1 0 0	0 0 1 1 1 0	0 1 1 1 1 1	0 0 1 1 1 1
	Q2	0 0 1 0 1 0	0 1 0 0 0 1	0 1 0 0 0 0	0 1 0 0 0 0
	Q3	0 1 0 0 0 1	0 1 0 0 0 0	0 1 0 0 0 0	0 1 0 0 0 0
	Q4	0 1 0 0 0 1	0 1 0 0 0 0	0 1 1 1 1 0	0 1 0 0 0 0
	Q5	0 1 1 1 1 1	0 1 0 0 0 0	0 1 0 0 0 0	0 1 0 0 1 1
	Q6	0 1 0 0 0 1	0 1 0 0 0 1	0 1 0 0 0 0	0 1 0 0 0 1
	Q7	0 1 0 0 0 1	0 0 1 1 1 0	0 1 1 1 1 1	0 0 1 1 1 1
0 0 1 x x 0	Q1	0 1 0 0 0 1	0 0 0 0 0 1	0 1 0 0 0 0	0 1 0 0 0 1
	Q2	0 1 0 0 0 1	0 0 0 0 0 1	0 1 0 0 0 0	0 1 0 0 0 1
	Q3	0 1 0 0 0 1	0 0 0 0 0 1	0 1 0 0 0 0	0 1 1 0 0 1
	Q4	0 1 1 1 1 1	0 0 0 0 0 1	0 1 0 0 0 0	0 1 0 1 0 1
	Q5	0 1 0 0 0 1	0 0 0 0 0 1	0 1 0 0 0 0	0 1 0 0 1 1
	Q6	0 1 0 0 0 1	0 1 0 0 0 1	0 1 0 0 0 0	0 1 0 0 0 1
	Q7	0 1 0 0 0 1	0 0 1 1 1 0	0 1 1 1 1 1	0 1 0 0 0 1
0 0 1 x x 1	Q1	0 0 1 1 1 0	0 1 0 0 0 1	0 1 0 0 0 1	0 0 1 1 1 0
	Q2	0 0 0 1 0 0	0 1 0 0 1 0	0 1 1 0 1 1	0 1 0 0 0 1
	Q3	0 0 0 1 0 0	0 1 0 1 0 0	0 1 0 1 0 1	0 1 0 0 0 1
	Q4	0 0 0 1 0 0	0 1 1 0 0 0	0 1 0 1 0 1	0 1 0 0 0 1
	Q5	0 0 0 1 0 0	0 1 0 1 0 0	0 1 0 0 0 1	0 1 0 0 0 1
	Q6	0 0 0 1 0 0	0 1 0 0 1 0	0 1 0 0 0 1	0 1 0 0 0 1
	Q7	0 0 1 1 1 0	0 1 0 0 0 1	0 1 0 0 0 1	0 0 1 1 1 0



NOTE: 1 = LOW: 0 = HIGH

FDR131Z2 BIT PATTERN AND FONT (continued)

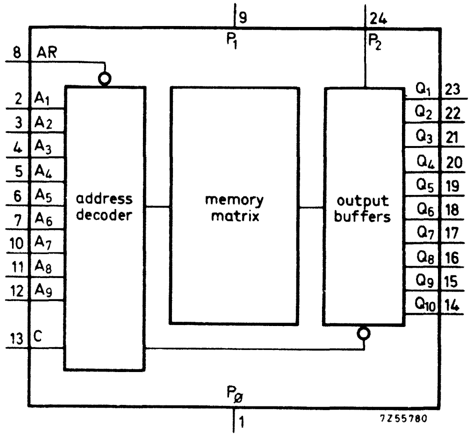
ASCII CHARACTER ADDRESS INPUTS b_6 b_5 b_4 b_3 b_2 b_1 / A_9 A_8 A_7 A_6 A_5 A_4	ROM OUTPUTS	COLUMN SELECT INPUTS A_1 0 1 0 1 0 1 / A_2 0 0 1 1 0 0 / A_3 0 0 0 0 1 1	A_1 0 1 0 1 0 1 / A_2 0 0 1 1 0 0 / A_3 0 0 0 0 1 1	A_1 0 1 0 1 0 1 / A_2 0 0 1 1 0 0 / A_3 0 0 0 0 1 1	A_1 0 1 0 1 0 1 / A_2 0 0 1 1 0 0 / A_3 0 0 0 0 1 1
x x →		00	01	10	11
1 0 0 x x 0	Q_1	0 0 0 0 0 0	0 0 1 0 1 0	0 0 0 1 0 0	0 0 1 0 0 0
	Q_2	0 0 0 0 0 0	0 0 1 0 1 0	0 0 1 1 1 1	0 1 0 1 0 0
	Q_3	0 0 0 0 0 0	0 0 1 0 1 0	0 1 0 1 0 0	0 1 0 1 0 0
	Q_4	0 0 0 0 0 0	0 0 0 0 0 0	0 0 1 1 1 0	0 0 1 0 0 0
	Q_5	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 1 0 1	0 1 0 1 0 1
	Q_6	0 0 0 0 0 0	0 0 0 0 0 0	0 1 1 1 1 0	0 1 0 0 1 0
	Q_7	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 1 0 0	0 0 1 1 0 1
1 0 0 x x 1	Q_1	0 0 0 1 0 0	0 0 1 0 1 0	0 1 1 0 0 0	0 0 0 1 0 0
	Q_2	0 0 0 1 0 0	0 0 1 0 1 0	0 1 1 0 0 1	0 0 0 1 0 0
	Q_3	0 0 0 1 0 0	0 1 1 1 1 1	0 0 0 0 1 0	0 0 0 1 0 0
	Q_4	0 0 0 1 0 0	0 0 1 0 1 0	0 0 0 1 0 0	0 0 0 0 0 0
	Q_5	0 0 0 1 0 0	0 1 1 1 1 1	0 0 1 0 0 0	0 0 0 0 0 0
	Q_6	0 0 0 0 0 0	0 0 1 0 1 0	0 1 0 0 1 1	0 0 0 0 0 0
	Q_7	0 0 0 1 0 0	0 0 1 0 1 0	0 0 0 0 1 1	0 0 0 0 0 0
1 0 1 x x 0	Q_1	0 0 0 1 0 0	0 0 0 1 0 0	0 0 0 0 0 0	0 0 0 0 0 0
	Q_2	0 0 1 0 0 0	0 1 0 1 0 1	0 0 0 0 0 0	0 0 0 0 0 0
	Q_3	0 1 0 0 0 0	0 0 1 1 1 0	0 0 0 0 0 0	0 0 0 0 0 0
	Q_4	0 1 0 0 0 0	0 0 0 1 0 0	0 0 0 0 0 0	0 0 0 0 0 0
	Q_5	0 1 0 0 0 0	0 0 1 1 1 0	0 0 0 1 0 0	0 0 0 0 0 0
	Q_6	0 0 1 0 0 0	0 1 0 1 0 1	0 0 0 1 0 0	0 0 0 0 0 0
	Q_7	0 0 0 1 0 0	0 0 0 1 0 0	0 0 1 0 0 0	0 0 0 1 0 0
1 0 1 x x 1	Q_1	0 0 0 1 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0
	Q_2	0 0 0 0 1 0	0 0 0 1 0 0	0 0 0 0 0 0	0 0 0 0 0 1
	Q_3	0 0 0 0 0 1	0 0 0 1 0 0	0 0 0 0 0 0	0 0 0 0 1 0
	Q_4	0 0 0 0 0 1	0 1 1 1 1 1	0 1 1 1 1 1	0 0 0 1 0 0
	Q_5	0 0 0 0 0 1	0 0 0 1 0 0	0 0 0 0 0 0	0 0 1 0 0 0
	Q_6	0 0 0 0 1 0	0 0 0 1 0 0	0 0 0 0 0 0	0 1 0 0 0 0
	Q_7	0 0 0 1 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0

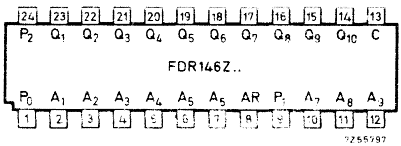


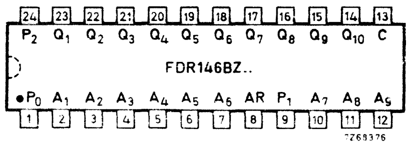
NOTE: 1 = LOW: 0 = HIGH

The FD family is a series of complex monolithic integrated circuits utilizing MOS P- channel enchancement mode technology.

READ ONLY MEMORY, 512 WORD, 10 BITS PER WORD







P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA				
Read access time	t_{ac}	max.	725	ns
Supply voltage	V_{P1}	−24 to	−28	V
Power dissipation	P_{tot}	typ.	300	mW
D.C. noise margin	M_H, M_L	>	1	V
Operating ambient temperature	T_{amb}	−55 to	+85	°C

PACKAGE OUTLINE

FDR146Z.. : 24 lead metal ceramic dual in-line (See General Section)
FDR146BZ.. : 24 lead plastic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDR146(B)Z is a monolithic 5120-bit, static operated, READ-only memory with a built-in output register. The contents is read into the register after an address READ pulse and the outputs remain steady until the next address READ pulse.
The 5120 bits are organized into 512 10-bit words, making the memory suitable for use in look-up tables, code connectors, message and logic function generators, and in micro-programmers with sufficient capacity for next instruction or flags. It can also be treated as 64 8x10 matrices for high-resolution character generators. The memory is programmed during manufacture with the aid of a pattern made to the customer's specifications.
Internal resistors at the input provide pull-up for TTL sources. For high speed operation these resistors should be shunted and one of the output configurations illustrated in the section on output buffers should be used.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0,5 to	−30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1,25	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminal P_1	$\pm I_{P1}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	100	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C; P_0 = grounded.

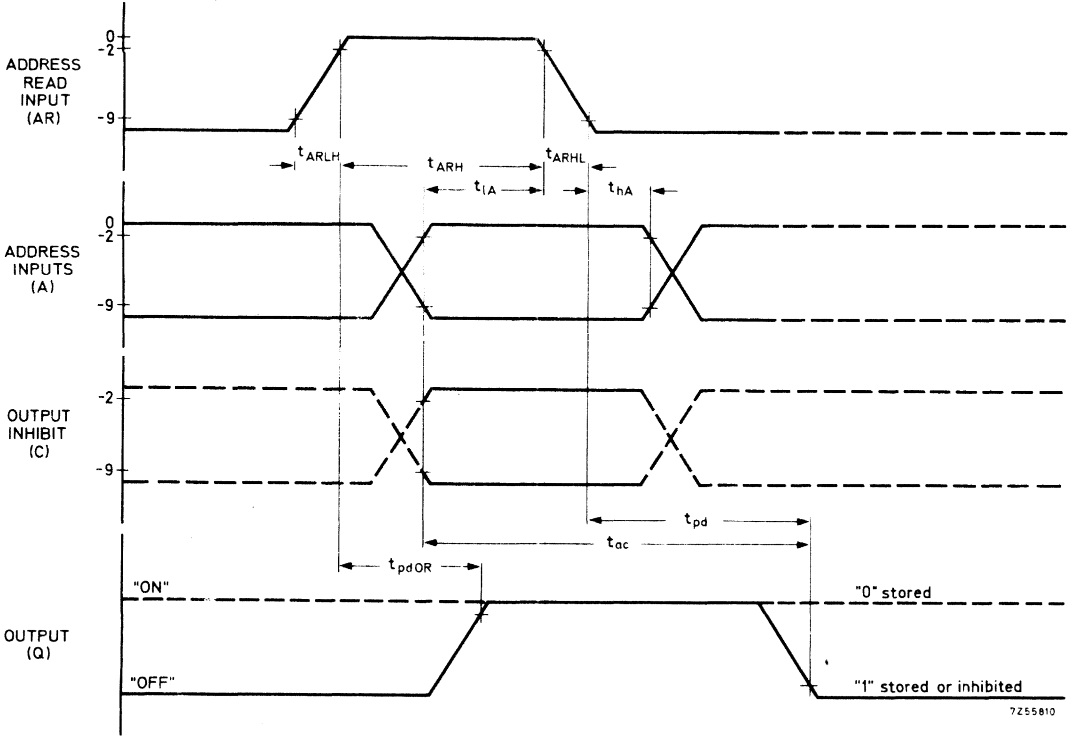
Electrical drive requirements	Symbol	min.	typ.	max.	conditions and references
Supply voltages					
P_1	$-V_{P1}$	24	-	28 V	
P_2	$-V_{P2}$	0	-	15 V	
Supply current at P_1					
	$-I_{P1}$	-	9	- mA	V_{P1} = -24 V; T_{amb} = 25°C
	$-I_{P1}$	-	-	18 mA	V_{P1} = -27 V; T_{amb} = 25°C
Logic levels					
(all inputs)					
HIGH	V_{AH}; V_{CH}; V_{ARH}	-2,0	-	+0,3 V	
LOW	V_{AL}; V_{CL}; V_{ARL}	-15,0	-12,0	-9 V	
Read rate	f_{AR}	0	-	1,33 MHz	$t_{ARLH} + t_{ARHL}$ = 50 ns
Address read pulse times					See interface circuit "a" on page 7
pulse width	t_{ARH}	0,2	-	100 µs	
rise time	t_{ARLH}	-	-	100 ns	
fall time	t_{ARHL}	-	-	100 ns	
address lead time	$t_{\ell A}$	200	-	- ns	
address hold time	t_{hA}	50	-	- ns	

CHARACTERISTICS (continued)

Test conditions: V_{P1} = −24 V to −28 V; V_{P2} = 0 to −15 V; T_{amb} = −55 to +85 °C

Electrical data	Symbol	min.	typ.	max.		conditions and refernces
Read access time	t_{ac}	–	–	750	ns	see timing diagram
Propagation delay	t_{pd}	–	–	500	ns	
Output reset delay	$t_{pd\,OR}$	75	–	400	ns	
Output currents						
"OFF" condition	$-I_Q$	–	–	167	µA	V_{P2} = 0; V_Q = −10 V; T_{amb} = 25 °C
"ON" condition	$-I_Q$	2,5	4,5	–	mA	V_{P1} = −23 V; V_{P2} = 0 V; V_Q = −2,5 V
Input capacitances						
Address input	C_A	–	3,5	4	pF	V_A = 0 V; f = 1 MHz
Address read input	C_{AR}	–	4	4,5	pF	V_{AR} = 0 V; f = 1 MHz
Output inhibit input	C_C	–	4,5	5	pF	
Input resistance						
(all inputs)	R_A;R_{AR};R_C	–	15	35	kΩ	between input and P_0
Output capacitance	C_Q	–	3,5	4,5	pF	V_Q = 0 V; f = 1 MHz

CHARACTERISTICS (continued)



Notes:

1. To enable the device the output inhibit input C should be HIGH during the specified time; to inhibit the device it should be LOW during that time.
2. The indicated points on the vertical axis are specified in the glossary of terms.

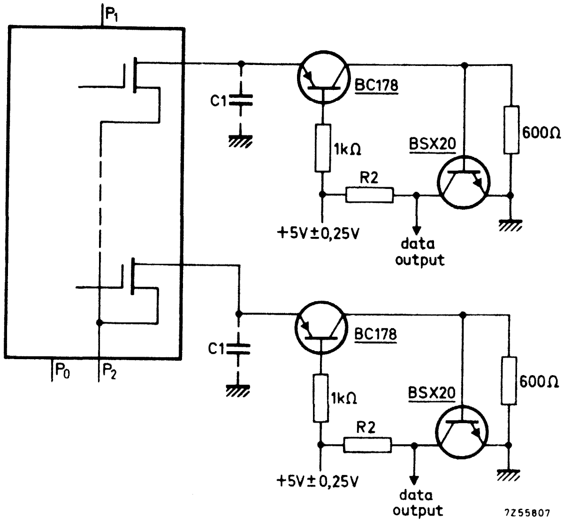
CHARACTERISTICS (continued)

Glossary of terms

1. Address read pulse width: t_{ARH}
   The time for which the address read pulse is HIGH: $V_{AR} \geq -2V$.
2. Address read pulse rise time: t_{ARLH}
   The time between the −9 V and −2 V voltage points as the read pulse goes from LOW to HIGH.
3. Address read pulse fall time: t_{ARHL}
   The time between the −2 V and −9 V voltage points as the read pulse goes from HIGH to LOW.
4. Output reset delay: t_{pdOR}
   After the AR pulse reaches HIGH, the time that elapses before the output reaches its "ON" state.
5. Address lead time: $t_{\ell A}$
   The time that the address and output inhibit signals must be valid before the start of the falling edge of the AR pulse.
6. Address hold time: t_{hA}
   The time that the address and output inhibit signals must be valid after the end of the falling edge of the AR pulse.
7. Propagation delay: t_{pd}
   The time between the end of the AR pulse and the output assumes its correct state.
8. Read access time: t_{ac}
   The time between the points, the address and output inhibit signals must be valid and the output assumes its correct state.

OUTPUT BUFFER DESCRIPTION

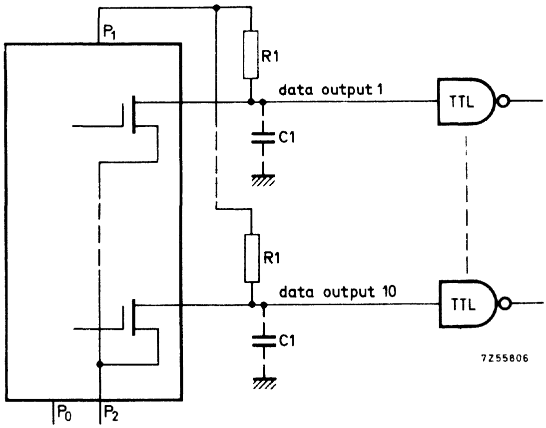
a. Current sense output interface



V_{P1} (V)	V_{P0} (V)	V_{P2} (V)	t_{ARH} (ns)	t_{ac} (ns)	cycle time (ns)	R2 (Ω)	load C1 (pF)	TTL fan-out
−12,5 to −13,5	+12,5 to +13,3	+7,0 to +8,0	> 200	< 725	< 750	> 150	< 100	20

OUTPUT BUFFER DESCRIPTION (continued)

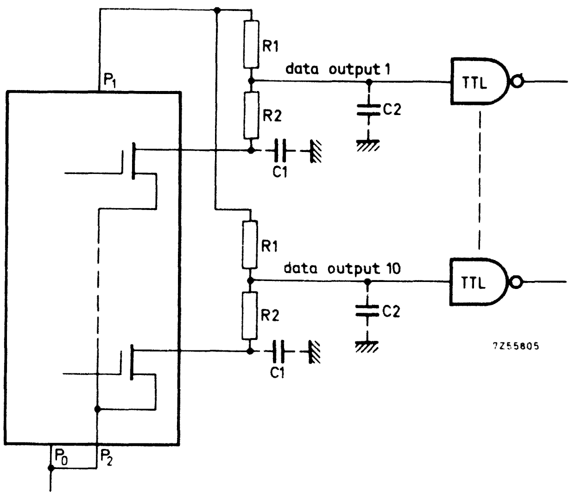
b. single resistor TTL interface



V_{P1} (V)	V_{P0} (V)	V_{P2} (V)	t_{ARH} (ns)	t_{ac} (ns)	cycle time (ns)	R1 (kΩ)	load C1 (pF)	TTL fan-out
-12,5 to -13,5	+12,5 to 13,5	+5,75 to +6,25	>200	<725	<750	6,8	<15	1
-11,5 to -13,5	+11,5 to 13,5	+5,75 to +6,25	>250	<725	<800	6,8	<15	1
-14,5 to -15,5	+ 9,5 to 10,5	+4,75 to +5,25	>250	<725	<800	8,2	<15	1

OUTPUT BUFFER DESCRIPTION (continued)

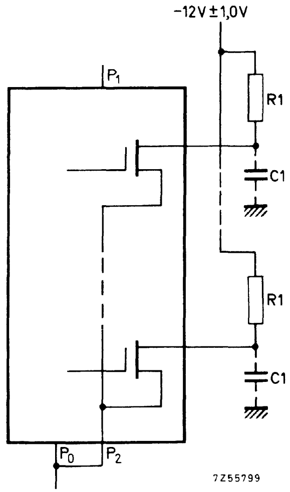
c. Two resistor TTL interface



V_{P1} (V)	V_{P0} (V)	t_{ARH} (ns)	t_{ac} (ns)	cycle time (ns)	R1 (kΩ)	R2 (kΩ)	load C1;C2 (pF)	TTL fan-out
-11,5 to -13,5	+11,5 to +13,5	>250	<725	<800	6,8	3,0	10	1
-12,5 to -13,5	+12,5 to +13,5	>200	<725	<750	6,8	3,0	10	1

OUTPUT BUFFER DESCRIPTION (continued)

d. MOS interface



V_{P1} (V)	V_{P0} (V)	V_{P2} (V)	t_{ARH} (ns)	t_{ac} (ns)	cycle time (ns)	R1 (kΩ)	C1 (pF)
−23,0 to −27,0	0	0	>250	< 825	<900	12	10

INPUT INTERFACE

Inputs A_1 to A_9, output inhibit C and address READ AR all have internal pull-up resistors to make them compatible with bipolar (TTL and DTL) circuits without requiring any additional components.

In the typical TTL-to-MOS interface shown below, V_{P1} is biased to −12 V, V_{P0} to +12 V, and the TTL gates to +5 V and ground. A TTL HIGH level at the gate input results in a MOS LOW level at the ROM input. When a TTL LOW level is initiated, the internal resistor R_i provides pull-up for the voltage rise of the TTL output. The external resistor R_S is for the purpose of improving rise time only. The gate can be any TTL device with 15 V output rating.

ROM input rise and fall times are dependent upon the total input capacitive load and the impedance of the TTL driving circuit during turn-off and turn-on respectively.

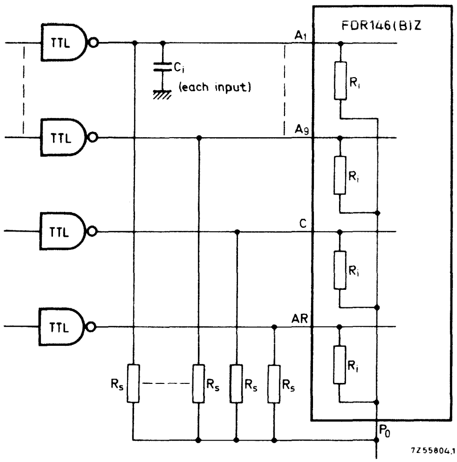
The rise time required for a 0 to 10 V transition is about 2 RC. Because of the relatively high value of R_i (35 kΩ max.), the rise time may approach 700 ns for a 10 pF load; to increase the speed at the input, shunt R_i with an external resistor.

$$\text{Since } t_{ARLH} = 2\,R_tC_i = 2\,\left(\frac{R_i R_S}{R_i + R_S}\right) C_i$$

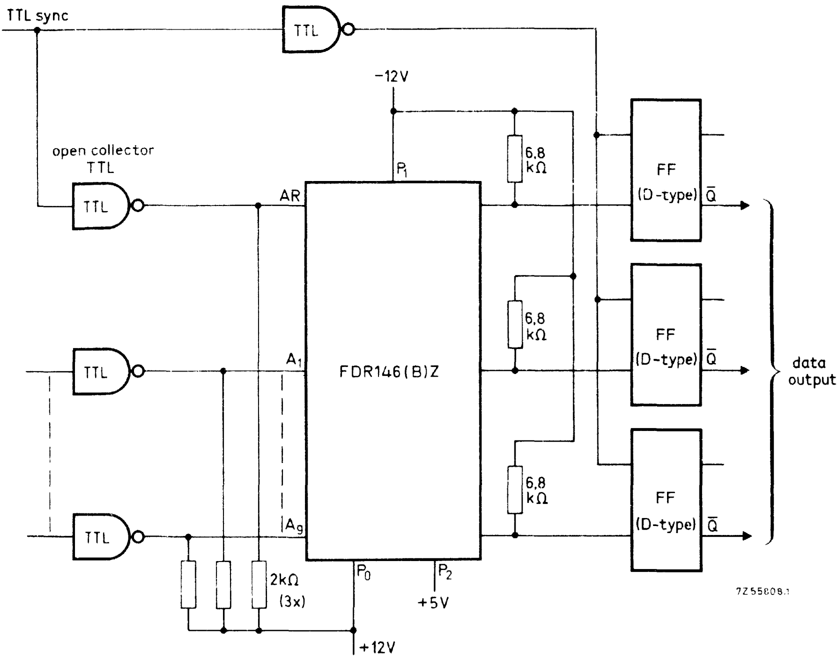
For a 50 ns rise time, R_t would equal 2,5 kΩ, so R_S = 2,8 kΩ.

The fall time is given by $t_{ARHL} \approx C_i \cdot V_p/I_{sink}$, where I_{sink} is 50 to 100 mA for the FJ family types, and V_p is the voltage transition. The values of R_i and R_S are not significant in the determination of fall time.

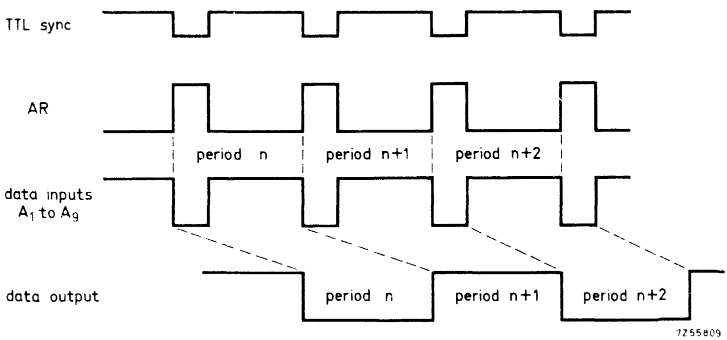
Assume the rise time of 700 ns to be as derived above for the address inputs. Allow 300 ns for the period $t_{\ell A} + t_{hA} + t_{ARHL}$. This indicates that for operating at cycle times greater than 1 μs with a new address available immediately after t_{hA}, no additional components are required at the input circuit. For operating at cycle times faster than 1 μs, the shunt resistor R_S is required.



APPLICATION INFORMATION

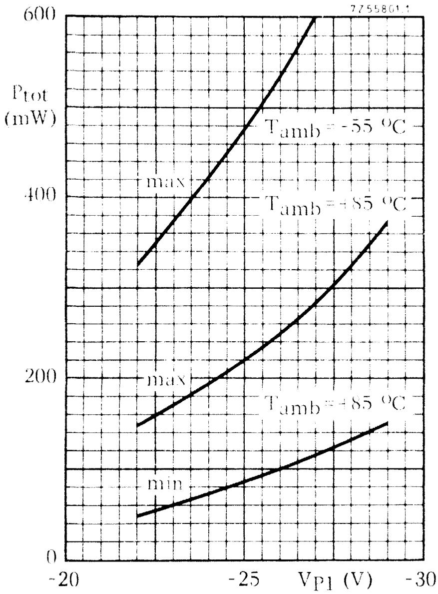


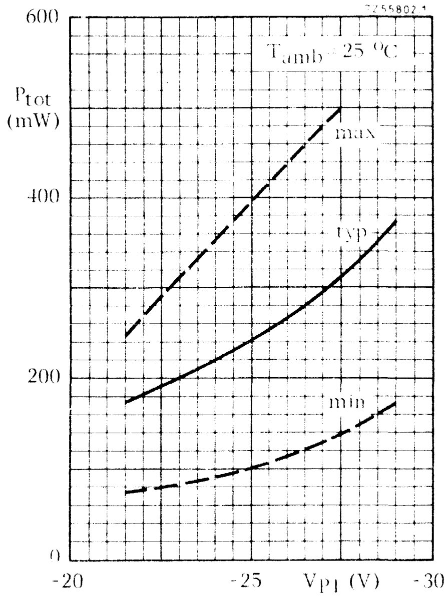
This circuit can be used to obtain NRZ outputs

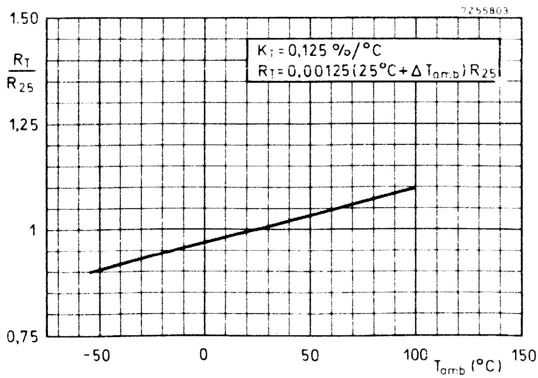


For this example, data stored in address during periods n, n + 1 and n + 2 have been arbitrarily to be "1", "0", "1" respectively.

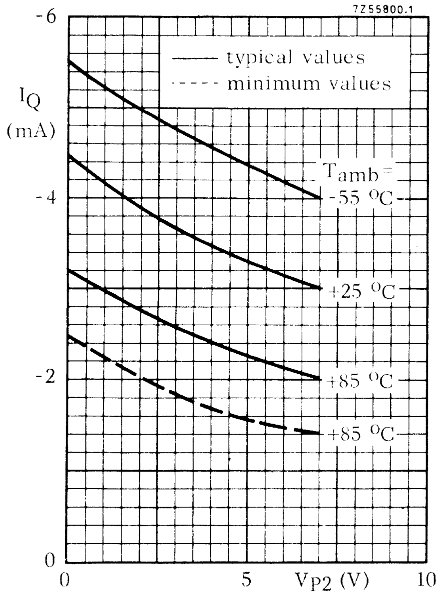
TYPICAL PERFORMANCE



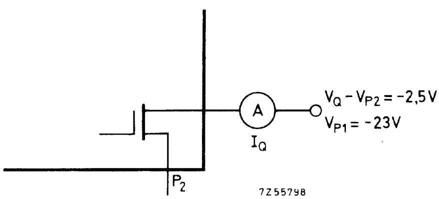




TYPICAL PERFORMANCE (continued)



Test circuit:



PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 17. Eight forms are needed for 512 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched cards are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customer's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made and the unique type number suffix is assigned.

Instruction for completing the forms

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

1. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid-out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

B. Address inputs

a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.

b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.

c) Bit 7, 8, and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1])
Memories of 256 words need 4 pages, of specifications.

d) Only ones(1 = "OFF")or zeros (0 = "ON") should be used in completing the form except where, a column is unused and is, therefore, left blank.

[1]) See example on page 17

p.t.o.

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN (continued)

2. Contents (data outputs)
   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 10 using only ones(1 = "OFF")and zeros (0 = "ON"), except where a column is unused and is, therefore, left blank.

3. Authorized signature

   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern FDR 146 ...

page of

AUTHORIZED SIGNATURE

CUSTOMER NAME:

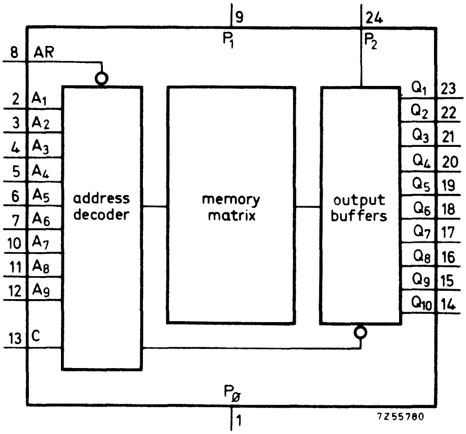
DATE

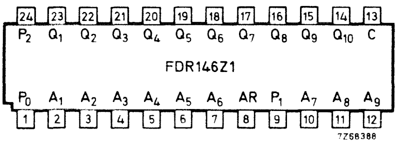
ADDRESS INPUTS	CONTENTS			
	00 OUTPUTS	01 OUTPUTS	10 OUTPUTS	11 OUTPUTS
9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1
1 2 3 4 5 6 7	8 9 10 11 12 13 14 15 16 17	18 19 20 21 22 23 24 25 26 27	28 29 30 31 32 33 34 35 36 37	38 39 40 41 42 43 44 45 46 47
X X 0 0 0 0				
X X 0 0 0 1				
X X 0 0 1 0				
X X 0 0 1 1				
X X 0 1 0 0				
X X 0 1 0 1				
X X 0 1 1 0				
X X 0 1 1 1				
X X 1 0 0 0				
X X 1 0 0 1				
X X 1 0 1 0				
X X 1 0 1 1				
X X 1 1 0 0				
X X 1 1 0 1				
X X 1 1 1 0				
X X 1 1 1 1				

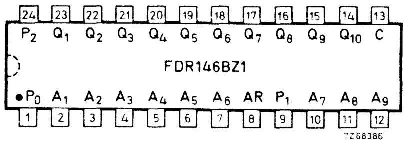
Note: 1 = "OFF"; 0 = "ON"

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enchancement mode technology.

STATIC CHARACTER GENERATOR
HIGH RESOLUTION UPPER CASE
(7 × 9 dot matrix; row scan system)







P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA				
Read access time	t_{ac}	max.	725	ns
Supply voltage	V_{P1}		−24 to −28	V
Power dissipation	P_{tot}	typ.	300	mW
D.C. noise margin	M_H, M_L	>	1	V
Operating ambient temperature	T_{amb}		−55 to +85	^oC

PACKAGE OUTLINE

FDR146Z1. : 24 lead metal ceramic dual in-line (See General Section)
FDR146BZ1. : 24 lead plastic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDR146(B)Z1 is a pre-programmed version of the FDR146(B)Z and contains 64 ASCII encoded symbols.
Each high resolution character is a 7 x 9 dot matrix organized for column scanning (7 columns with 9 parallel output lines).
The input code is 6-bit ASCII. The 3-bit column code is internally decoded on the chip.
Access times of 725 ns or better are achievable by utilizing the appropriate output configuration.

RATINGS

CHARACTERISTICS

OUTPUT BUFFER DESCRIPTION

For this information see data sheets of FDR146(B)Z

CHARACTER GENERATOR ORGANIZATION

The FDR 146(B) Z 1 is primarily intended for generation of high resolution character fonts for vertical scan displays.

Each 63 bit character is composed of 7 distinct 9-bit columns. One of the 64 characters is selected by a 6-bit address applied to inputs A_5, A_6, A_7, A_8, A_9 and A_1 corresponding to the ASCII code bits b_6 to b_1 respectively.

The particular 9-bit column is determined by the 3-bit address applied to address inputs A_2, A_3 and A_4 (column SELECT inputs).

After seven successive column addresses, the entire character is completed. The 7 x 9 font is fitted to an 8 x 10 matrix, with column address 000 programmed with all zeros to provide character space and line space. Other usefull applications include a low speed horizontal scan usage (as in line printers) requiring high resolution. The technique involved to rotate the character is illustrated in the APPLICATION INFORMATION on page 5.

Example

In this example, with the ASCII character address fixed, the column select inputs are sequentially altered to produce one complete character of 8 successive columns. After 8 sequential binary column select iterations, the character address is changed and the column select procedure repeated.

All the 0 column select input addresses produce a space column.

Column SELECT inputs	A_2	0 1 0 1 0 1 0 1	0 1 0 1 0 1 0 1	0 1 0 1 0 1 0 1
	A_3	0 0 1 1 0 0 1 1	0 0 1 1 0 0 1 1	0 0 1 1 0 0 1 1
	A_4	0 0 0 0 1 1 1 1	0 0 0 0 1 1 1 1	0 0 0 0 1 1 1 1

ASCII character address	column 0 1 2 3 4 5 6 7	ASCII character address	column 0 1 2 3 4 5 6 7	ASCII character address	column 0 1 2 3 4 5 6 7	row
for "R" applied to b_6 to b_1 010010	0 1 1 1 1 1 1 0	for "O" applied to b_6 to b_1 001111	0 0 0 1 1 1 0 0	for "M" applied to b_6 to b_1 001101	0 1 1 0 0 0 1 1	→ 10
	0 1 0 0 0 0 0 1		0 0 1 0 0 0 1 0		0 1 0 1 0 1 0 1	→ 9
	0 1 0 0 0 0 0 1		0 1 0 0 0 0 0 1		0 1 0 0 1 0 0 1	→ 8
	0 1 0 0 0 0 0 1		0 1 0 0 0 0 0 1		0 1 0 0 1 0 0 1	→ 7
	0 1 1 1 1 1 1 0		0 1 0 0 0 0 0 1		0 1 0 0 0 0 0 1	→ 6
	0 1 0 0 1 0 0 0		0 1 0 0 0 0 0 1		0 1 0 0 0 0 0 1	→ 5
	0 1 0 0 0 1 0 0		0 1 0 0 0 0 0 1		0 1 0 0 0 0 0 1	→ 4
	0 1 0 0 0 0 1 0		0 0 1 0 0 0 1 0		0 1 0 0 0 0 0 1	→ 3
	0 1 0 0 0 0 0 1		0 0 0 1 1 1 0 0		0 1 0 0 0 0 0 1	→ 2
	0 0 0 0 0 0 0 0		0 0 0 0 0 0 0 0		0 0 0 0 0 0 0 0	→ 1

CHARACTER FONT AND INPUT CODE

ASCII INPUT ADDRESS	$b_3b_2b_1$ 000	001	010	011	100	101	110	111
$b_6b_5b_4$ 000	@	A	B	C	D	E	F	G
001	H	I	J	K	L	M	N	O
010	P	Q	R	S	T	U	V	W
011	X	Y	Z	[	\	]	^	_
100		!	"	#	$	%	&	'
101	(	)	*	+	,	-	.	/
110	0	1	2	3	4	5	6	7
111	8	9	:	;	<	=	>	?

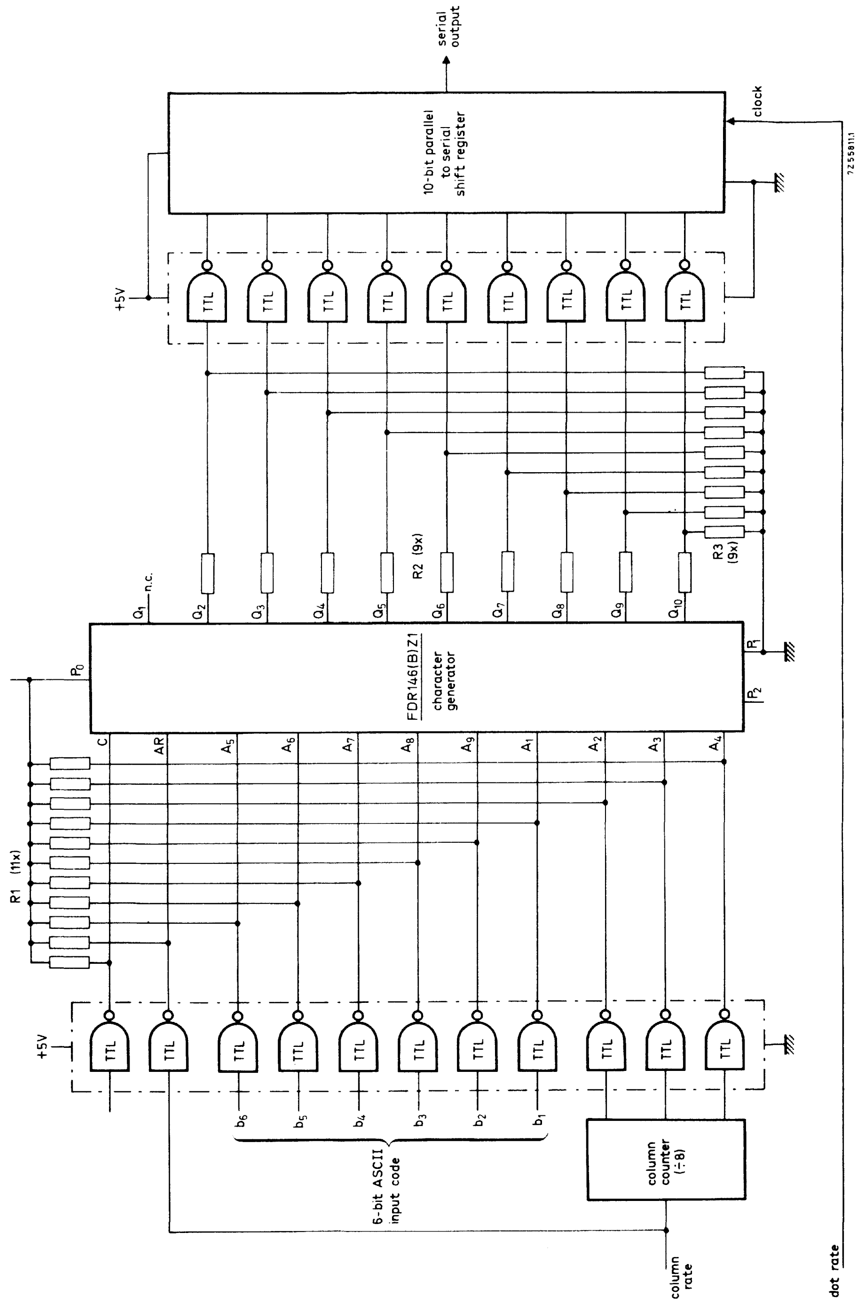
APPLICATION INFORMATION

Vertical column scanning (see circuit on page 6)

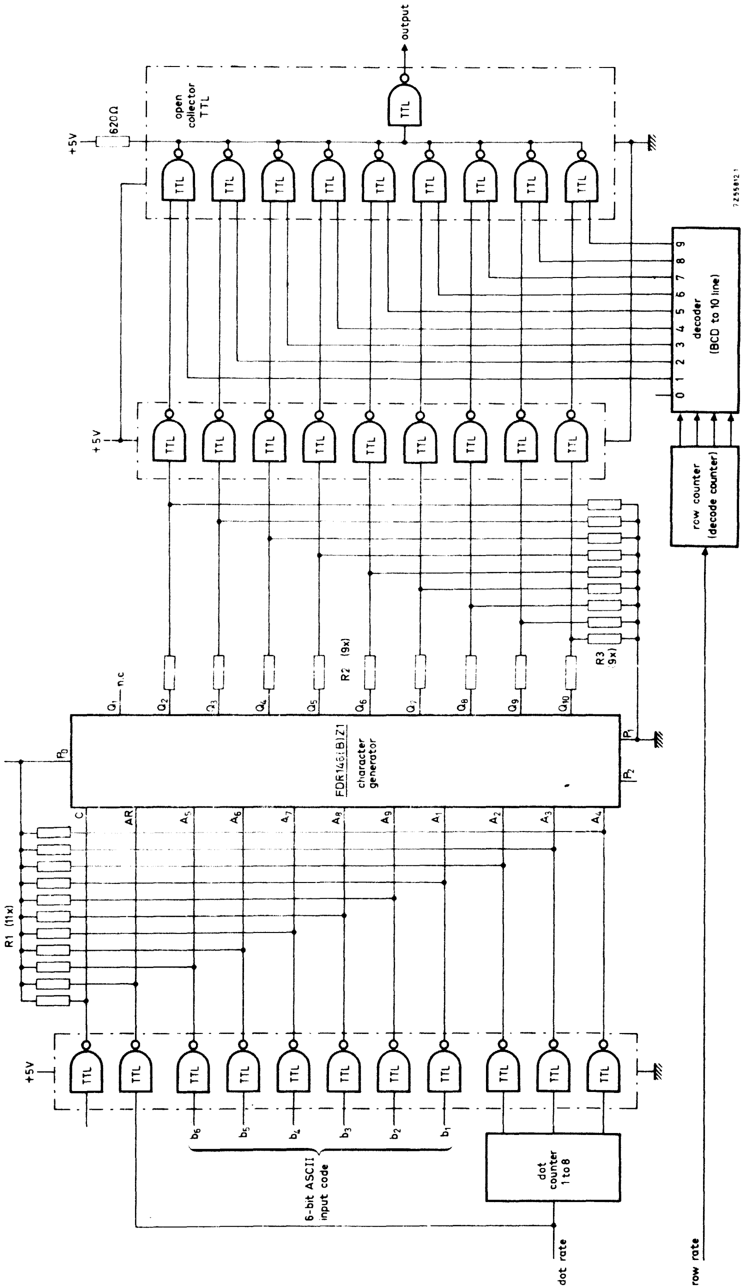
At a given ROM input address (an ASCII code plus the column code) nine parallel bits are detected, representing one column of a character. Depending upon the application, the entire column may be displayed at once, or as in the case of Z axis modulation of a single beam, it is necessary to convert the nine parallel bits to a single train of serial bits.
The "two resistor" interface is only one of several interface techniques that may be employed (see also FDR146(B)Z data sheet).

Low speed horizontal row scanning (see circuit on page 7)

For applications such as electronic printing in line increments this technique will rotate a pre-programmed vertical scan character font to one with a horizontal scan orientation. Essentially, the roles of the dot rate and the row rate have been interchanged. Again, the "two resistor" interface is only one of several interface techniques that may be employed.
For any given ROM address, only one bit is detected and is in the row determined by the state of the counter. To generate one complete row of information, the row counter holds while the dot counter scans the full row. This scan is repeated for each of the ten rows to generate a complete character. The scan time for one row is increased by the time required to address eight dot rows. Thus, for a device with a 700 ns cycle time, it would require 5.6 μs to complete the row of that character, which is the upper limit for this technique. The outputs of the gates are wired-OR, to provide one line out and to eliminate the parallel-to-serial shift register.



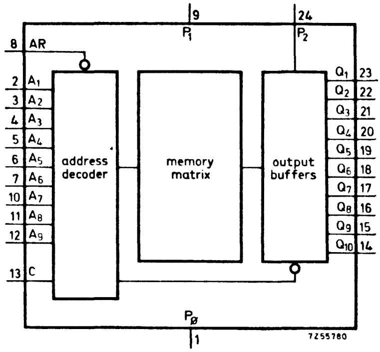
Vertical column scanning (see page 5)

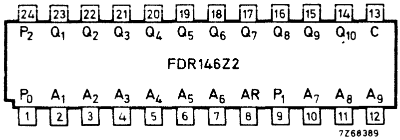


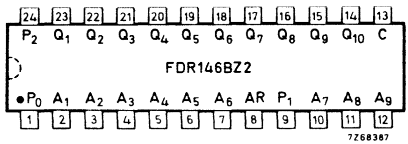
Low speed horizontal row scanning (see also page 5)

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enchancement mode technology.

STATIC CHARACTER GENERATOR
UPPER AND LOWER CASE
(5 × 7 dot matrix; row scan system)







P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA				
Read access time	t_{ac}	max.	725	ns
Supply voltage	V_{P1}		−24 to −28	V
Power dissipation	P_{tot}	typ.	300	mW
D.C. noise margin	M_H, M_L	>	1	V
Operating ambient temperature	T_{amb}		−55 to +85	°C

PACKAGE OUTLINE

FDR146Z2. : 24 lead metal ceramic dual in-line (See General Section)
FDR146BZ2.: 24 lead plastic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDR 146(B) Z2 is a pre-programmed version of the FDR146Z and intended for use as character generator in 5 x 7 dot matrix displays, where the full 7-bit ASCII character set is required.
128 characters are stored in the FDR 146(B) Z2, viz. the upper and lower case characters and a pictorial representation of the control codes.
The character generator is organized for row scan, i.e. when a 7-bit ASCII code and a 3-bit row code is applied, the five bits belonging to one horizontal row of the character font appear at the outputs.
Access times of 725 ns or better are achievable by utilizing the appropriate output configuration.

RATINGS

CHARACTERISTICS

OUTPUT BUFFER DESCRIPTION

For this information see data sheets of FDR 146(B) Z

CHARACTER FONT
AND INPUT CODE

b7 b6 b5 → / b4 b3 b2 b1	000	001	010	011	100	101	110	111
0000	NUL	DLE		0	@	P	`	p
0001	SOH	DC1	!	1	A	Q	a	q
0010	STX	DC2	"	2	B	R	b	r
0011	ETX	DC3	#	3	C	S	c	s
0100	EOT	DC4	$	4	D	T	d	t
0101	ENQ	NAK	%	5	E	U	e	u
0110	ACK	SYN	&	6	F	V	f	v
0111	BEL	ETB	'	7	G	W	g	w
1000	BS	CAN	(	8	H	X	h	x
1001	HT	EM	)	9	I	Y	i	y
1010	LF	SUB	*	:	J	Z	j	z
1011	VT	ESC	+	;	K	[	k	{
1100	FF	FS	,	<	L	\	l	|
1101	CR	GS	-	=	M	]	m	}
1110	SO	RS	.	>	N	^	n	~
1111	SI	US	/	?	O	_	o	▒

APPLICATION INFORMATION

To use the FDR 146(B) Z2 as a character generator the ASCII code of the character to be displayed should be applied to the inputs A_4 to A_9 with the following correspondence:

ASCII bit	address input
b_1	A_4
b_2	A_5
b_3	A_6
b_4	A_7
b_5	A_8
b_6	A_9

Negative logic is assumed for the inputs (HIGH = 0; LOW = 1).

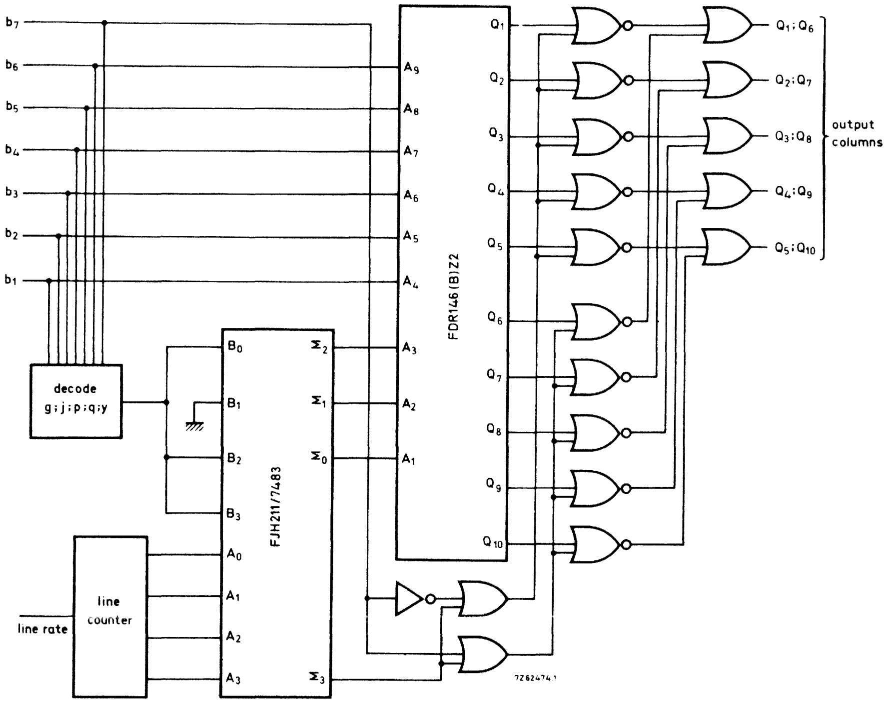
ASCII bit b_7 must be used to select between the outputs Q_1 to Q_5 or Q_6 to Q_{10} (See example on page 5).
The row select code should be applied to the inputs A_1 to A_3 (A_1 being the least significant bit).
The characters are stored in rows 1 to 7, row 0 contains blanks (see example below).
The figure on page 5 shows the block diagram of a character generator system incorporating a "descender" circuit, with which the lower case g, j, p, q and y can be lowered two rows. For this purpose an adder circuit is inserted between the row counter and the READ ONLY MEMORIES.
When a lower case g, j, p, q or y is detected a binary 2 is subtracted from the row number (actually the binary number 14 is added), which causes the character to be displayed two rows lower.
The output $\Sigma 3$ of the adder is used to blank all outputs in order to avoid a repeated display of the character during rows 9 and 10 in the "normal" position, or during rows 0 and 1 in the "descended" position.

ROM ORGANIZATION

ROW SELECT INPUTS A_3, A_2, A_1	row	ASCII CHARACTER ADDRESS FOR A, b_7 to b_1 1000001		ASCII CHARACTER ADDRESS FOR b, b_7 to b_1 1100010		ASCII CHARACTER ADDRESS FOR c, b_7 to b_1 1100011		ASCII CHARACTER ADDRESS FOR D, b_7 to b_1 1000100
0 0 0	0	0 0 0 0 0	→	0 0 0 0 0	→	0 0 0 0 0	→	0 0 0 0 0
0 0 1	1	0 0 1 0 0	→	1 0 0 0 0	→	0 0 0 0 0	→	1 1 1 1 0
0 1 0	2	0 1 0 1 0	→	1 0 0 0 0	→	0 0 0 0 0	→	1 0 0 0 1
0 1 1	3	1 0 0 0 1	→	1 1 1 1 0	→	0 1 1 1 1	→	1 0 0 0 1
1 0 0	4	1 0 0 0 1	→	1 0 0 0 1	→	1 0 0 0 0	→	1 0 0 0 1
1 0 1	5	1 1 1 1 1	→	1 0 0 0 1	→	1 0 0 0 0	→	1 0 0 0 1
1 1 0	6	1 0 0 0 1	→	1 0 0 0 1	→	1 0 0 0 0	→	1 0 0 0 1
1 1 1	7	1 0 0 0 1	→	1 1 1 1 0	→	0 1 1 1 1	→	1 1 1 1 0

In this example, with the row select input address fixed, the ASCII character addresses are sequentially altered to produce one line of four different characters, left to right. After 8 sequential binary row select iterations, using the same character address sequence, the complete row of characters is formed, including a space line.

APPLICATION INFORMATION (continued)



b_7 = logic LOW, selects Q_6 to Q_{10}

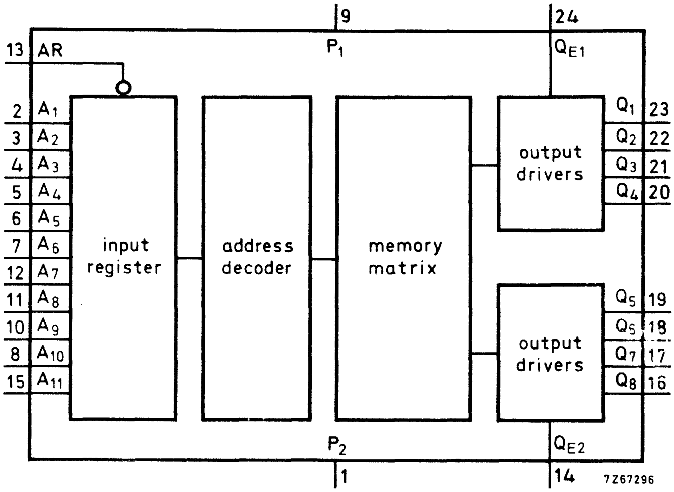
Block diagram of 128ASCII symbol character generator

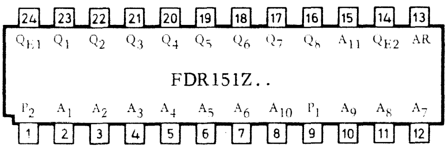
Note:

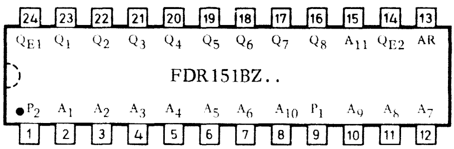
With a separate additional input on the counter, one could also utilize any of the characters as subscripts.

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

STATIC READ ONLY MEMORY, 2048 WORDS, 8 BITS PER WORD







P_2 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA

Read access time	t_{ac}	<	1, 2	μs
Supply voltages	V_{P1}		−11, 4 to −12, 6	V
	V_{P2}		+4, 75 to +5, 25	V
Power dissipation per bit at V_{P1} = −12 V	P_{tot}	typ.	32	μW
Ambient temperature	T_{amb}		0 to +70	°C

PACKAGE OUTLINE

FDR151Z.. : 24 lead metal ceramic dual in-line (See General Section)
FDR151BZ.. : 24 lead plastic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDR151(B)Z is a monolithic 16 384-bit, static operated, READ-only memory utilizing low voltage MOS enhancement mode P-channel technology.
When the address is read into the ROM, all outputs appear and remain in a steady state until a new address is read. Full address decoding is performed on chip. The 16 384 bits are organized as 2048 addresses with 8 output lines; its size enhances usage in any high density, fixed memory application such as logic function generation or micro-programming. The organization can also be considered as 128 8 x 16 matrices, particularly suitable for high resolution character generation. Programming of the device is accomplished via the use of one custom mask during fabrication.
Internal resistors at the input provide pull-up for direct TTL compatibility.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs and supply terminals		+0,25 to −18	V
Power dissipation at T_{amb} = 25 °C	P_{tot}	max. 1,25	W
Operating ambient temperature	T_{amb}	0 to +70	°C
Junction temperature	T_j	max. 150	°C
Storage temperature	T_{stg}	−65 to +150	°C

THERMAL RESISTANCE

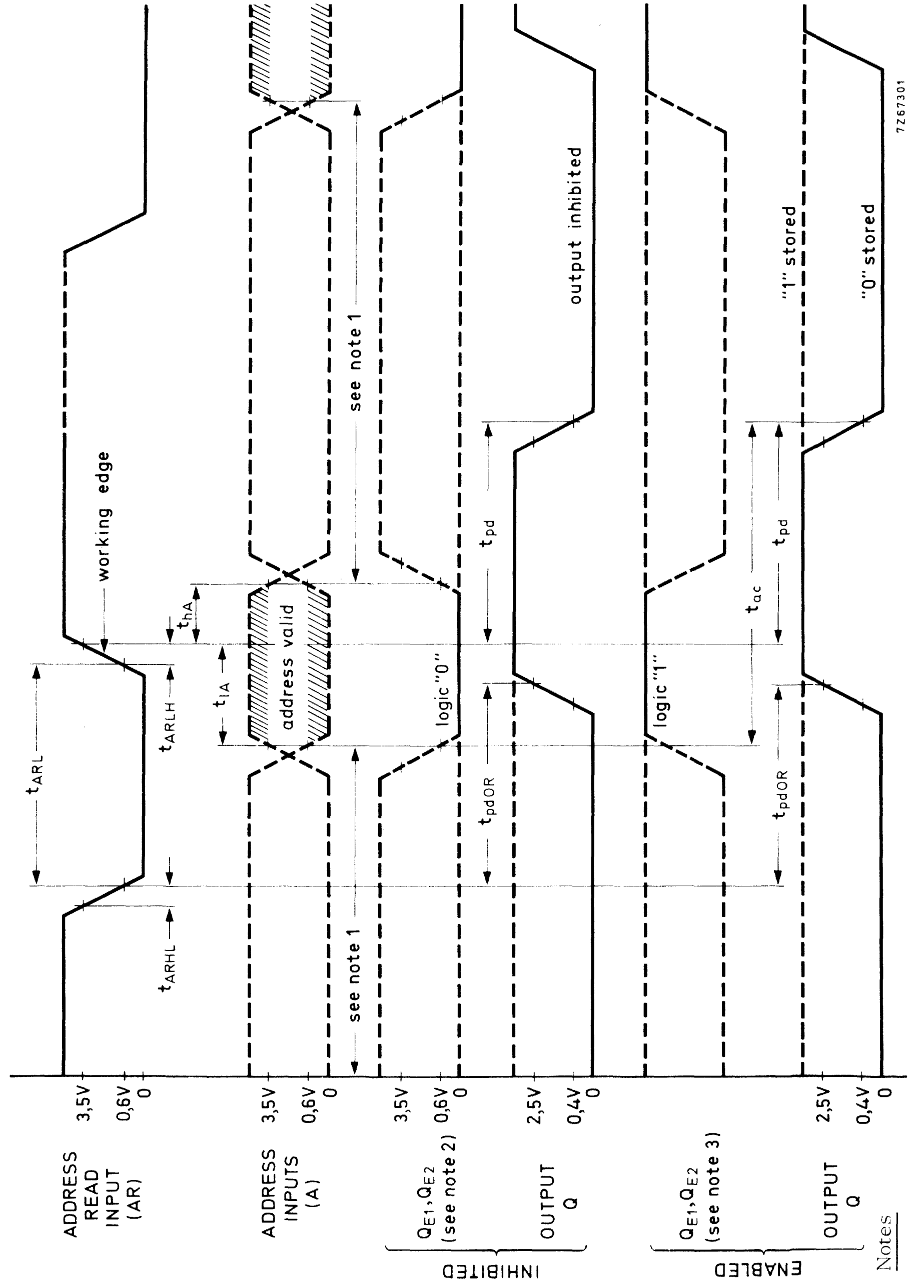
From junction to ambient	$R_{th\ j\text{-}a}$	= 100	°C/W

CHARACTERISTICS at T_{amb} = 0 to +70 °C; V_{P1} = −11,4 to −12,6 V; V_{P2} = +4,75 to 5,25 V

	Symbol	min.	typ.	max.		conditions
Drive requirements						
Supply currents	I_{P1}	–	−22	−30	mA	V_{P1} = −12,6 V;
	I_{P2}	–	22	30	mA	V_{P2} = +5,25 V
Logic levels						
address read input						
HIGH (see note 1)	V_{ARH}	V_{P2}-1,5	–	V_{P2}	V	
LOW	V_{ARL}	V_{P2}-17	–	+0,6	V	
address input						
HIGH (see note 1)	V_{AH}	V_{P2}-1,5	–	V_{P2}	V	
LOW	V_{AL}	V_{P2}-17	–	+0,6	V	
output enable						
HIGH (see note 1)	V_{QEH}	V_{P2}-1,5	–	V_{P2}	V	
LOW	V_{QEL}	V_{P2}-17	–	+0,6	V	
Timing information						
Address read times						
pulse duration	t_{ARL}	0,95	–	100	µs	See timing diagram on page 4 and glossary of terms on page 5
rise time	t_{ARLH}	–	–	100	ns	
fall time	t_{ARHL}	–	–	100	ns	
Address lead time	$t_{\ell A}$	500	–	–	ns	
Address hold time	t_{hA}	200	–	–	ns	
Read cycle time	t_{RC}	–	–	1700	ns	
Read access time	t_{ac}	–	–	1225	ns	
Propagation delay	t_{pd}	–	–	700	ns	
Output reset delay	t_{pdOR}	200	–	800	ns	
Electrical data						
Output logic levels						
HIGH	V_{QH}	2,5	–	–	V	TTL interface;
LOW	V_{QL}	–	–	0,4	V	I_{sink} ≤ 1,6 mA
HIGH	V_{QH}	–	–	−1,5	V	MOS interface; 12 kΩ to −17 V;
LOW	V_{QL}	−10	–	–	V	V_{P2} = 0; V_{P1} = −17 V
Address input capacitance	C_A	–	3,5	4	pF	0 V bias; f = 1 MHz
Address read input capacitance	C_{AR}	–	4	4,5	pF	0 V bias; f = 1 MHz
Address, output enable address read input resistance	R_A; R_{QE}; R_{AR}	3	–	9	kΩ	from input to P_2
Output capacitance	C_Q	–	3,5	4,5	pF	0 V bias; f = 1 MHz

[1]) Direct compatibility for TTL logic "1" (HIGH state) output voltage levels is provided by internal pull-up resistors connected to P_2.

TIMING DIAGRAM



Notes

1. Address may change for this time.
2. Output enable is logic "0" during address valid.
3. Output enable is logic "1" during address valid.

GLOSSARY OF TERMS (see page 4)

1. Address read pulse duration: t_{ARL}

   The time for which the address read pulse is LOW.

2. Address read pulse rise time: t_{ARLH}

   The time between the 0,6 V and 3,5 V voltage points as the address read pulse goes from LOW to HIGH.

3. Address read pulse fall time: t_{ARHL}

   The time between the 3,5 V and 0,6 V voltage points as the address read pulse goes from HIGH to LOW.

4. Propagation delay: t_{pd}

   The time between completion of the AR pulse until the output becomes valid.

5. Read cycle time: t_{RC}

   The read cycle time is the period between successive address read (AR) pulses. The minimum cycle time is determined by the sum of the AR pulse width, propagation delay, and the rise and the fall times of the AR pulse.
   $t_{ARLmin} + t_{pdmax} + t_{ARHL} + t_{ARLH}$, where $t_{ARHL} + t_{ARLH} = 50$ ns.

6. Read access time: t_{ac}

   The time required for the output to become valid after the address has become valid. The access time is defined as: $t_{\ell Amin} + t_{pdmax} + t_{ARLH}$, where $t_{ARLH} = 25$ ns.

7. Address lead time: $t_{\ell A}$

   The minimum time required for the address input to the valid prior to the rising edge of the AR pulse.

8. Address hold time: t_{hA}

   The minimum time required for the address input to remain valid after the rising edge of the AR pulse.

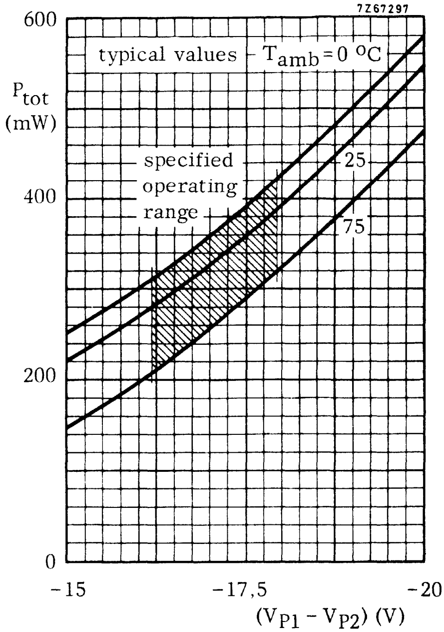
9. Output reset delay: t_{pdOR}

   After the AR pulse reaches LOW, the time that elapses before the output reaches its logic "1" state.

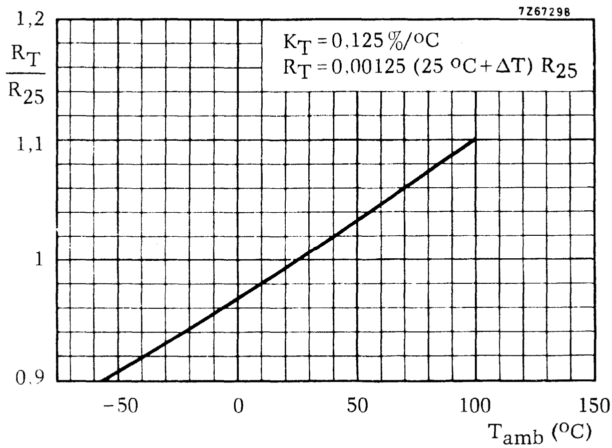
Note

Entry of data is caused by the rising edge (from LOW to HIGH) of the address read (AR) pulse, provided a valid, unchanging address is present throughout the period "address valid".

TYPICAL PERFORMANCE



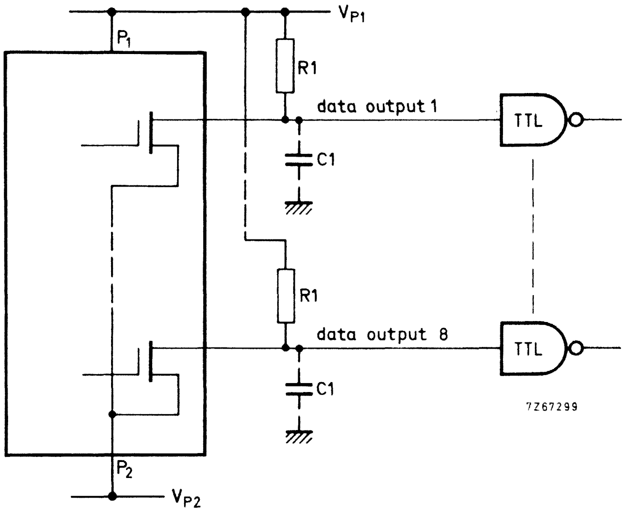
Power dissipation versus supply voltage



Variation of input resistance with temperature

OUTPUT BUFFER DESCRIPTION

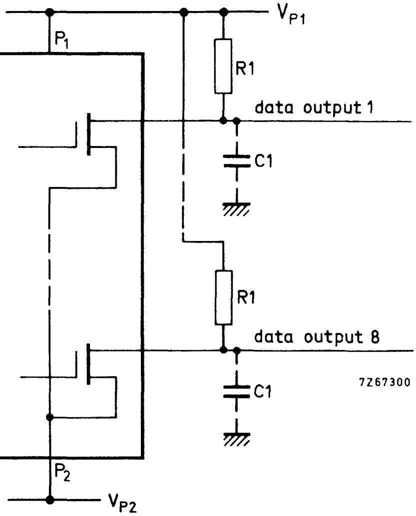
1. Single resistor TTL interface



V_{P1} (V)	V_{P2} (V)	t_{ARL} (ns)	t_{ac} (μs)	cycle time (μs)	R1 (kΩ)	load C1 (pF)	TTL fan-out
-11,4 to -12,6	+4,75 to +5,25	> 950	< 1,22	< 1,70	6,8	15	1

OUTPUT BUFFER DESCRIPTION (continued)

2. MOS interface



V_{P1} (V)	V_{P2} (V)	t_{ARL} (ns)	t_{ac} (µs)	cycle time (µs)	R1 (kΩ)	C1 (pF)
−16,2 to −17,9	0	> 950	< 1,22	< 1,70	12	10

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To order the FDR151(B)Z.. with a special bit pattern, customers should make use of a deck of 128 standard 80-column computer cards. The punched cards will enable us to transfer any desired bit pattern into a standard ROM without error.
After receipt of the cards our procedure is as follows:

1. The punched cards are incorporated in a computer program that originates the following:
   - a matching print-out for pattern verification
   - a full scale plot of all ones and zeros for custom mask generation
   - a control tape for programming final electrical testing of the customer's ROM.
2. The computer print-out is checked against the original cards submitted; a copy is also sent to the customer for his verification and signature.
3. Upon receipt of the customer's signed verification, full scale masks embodying the desired pattern are made.

Instruction for completing the cards

For this very large Read Only Memory the data to be stored in the ROM is submitted by means of computer cards in order to avoid any hand transfer of large patterns.
To reduce the number of cards to be handled, information is recorded in octal notation.

The required punching format is described below. All addresses must be included with their outputs defined. That is, no assumptions are made regarding the bit configurations of undefined outputs. Therefore the customer must submit cards defining the entire ROM contents, even though part or portions of the ROM may be unused (zeros).

DATA CARD FORMAT

1. The ADDRESS INPUTS and CONTENTS (outputs)

   Each card of the ROM bit pattern card-deck is used for 16 consecutive output-words preceeded by an initial address (see below).

1A. Address inputs

   a. There are eleven address inputs A_1 to A_{11}; A_1 corresponds to the least significant bit of the binary address code and A_{11} to the most significant.
   b. In converting binary to octal, bear in mind that the least significant octal digit corresponds to address inputs A_3 A_2 A_1, and the most significant to inputs A_{11} A_{10}; e.g.

address inputs

	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1
binary	1	0	0	1	0	0	1	1	1	1	0
octal	2			2			3			6	

Thus 2236 is the 4-digit octal number representing the input address 10010011110.

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN (continued)

1B. Contents (data output)

a. There are eight outputs Q_1 to Q_8: Q_1 corresponds to the right-hand bit.
b. In converting the desired outputs to octal notation, take care that outputs Q_3 Q_2 Q_1 correspond to the least significant octal digit, and outputs Q_8 Q_7 to the most significant: e.g.

	outputs							
	Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
binary	0	1	1	0	1	0	0	1
octal	1			5			1	

Thus 151 is the 3-digit octal number representing the output contents 01101001.

2. Card punching

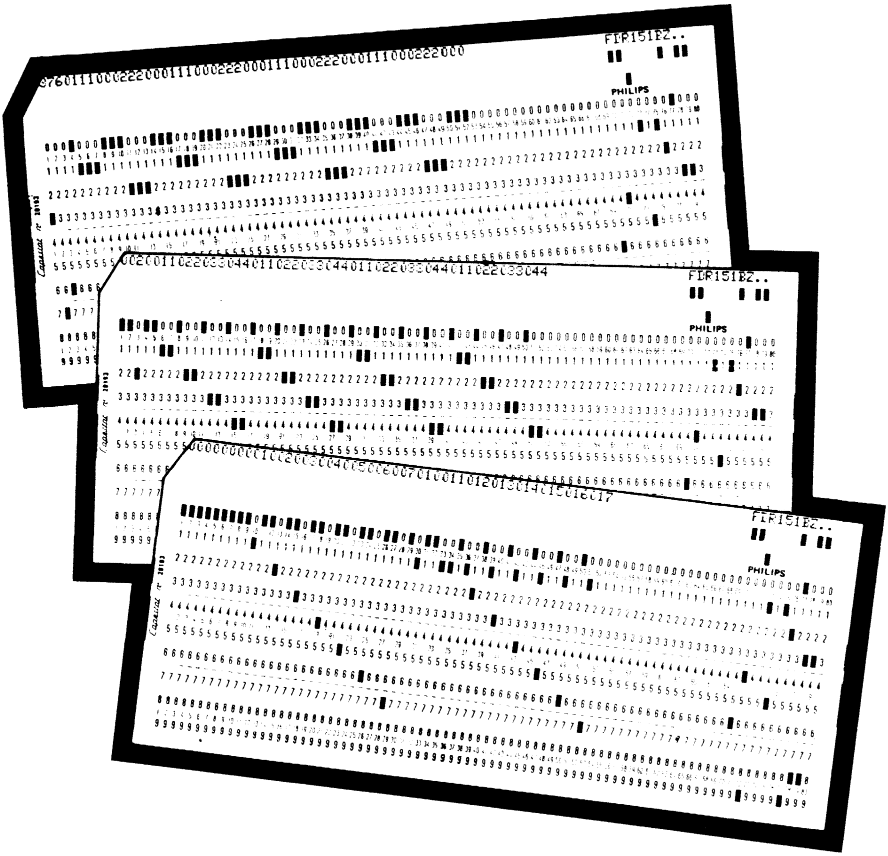
Each card is to be punched as folows:

card column No.	card contents
1 - 4	Punch a 4-digit octal number representing the input address for the first of the 16 output words appearing on this card. This is the initial address.
5 - 7	Punch a 3-digit octal number representing the outputs for the initial address.
8 - 10	Punch a 3-digit octal number representing the outputs for the initial address + 1.
11 - 13	Punch a 3-digit octal number representing the outputs for the initial address + 2.
↓	↓
50 - 52	Punch a 3-digit octal number representing the outputs for the initial address + 15.
70 - 79	The unique number assigned to this ROM pattern (obtainable from the local Philips representative). The customer may punch this number into the card or leave these columns blank, to be punched later by the manufacturer.

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN (continued)

Each card, therefore, carries the initial input address (in octal) for the 16 output words contained on that card, the 16 output words themselves (in octal) and possibly the unique ROM number.
Cards must be provided for all possible sequential locations (blocks of 16).
The 2048 word ROM FDR151(B)Z.. therefore requires 128 cards, with all 16 output words defined on each card.

Below an example of the first, second and last card of a deck.

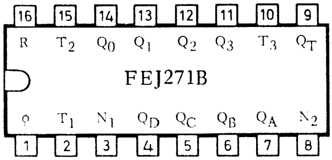


MOS FE family

FEJ271B	quadruple decade COUNTER/REGISTER
FEY101B	analogue/digital CONVERTER logic

The FE family is a series of monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

QUADRUPLE DECADE COUNTER/REGISTER



QUICK REFERENCE DATA				
Supply voltage	V_N		-24 ± 1,5	V
Operating ambient temperature	T_{amb}		0 to +75	^oC
Maximum operating frequency	f		1	MHz
Power consumption	P_{tot}	typ.	140	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section)

GENERAL DESCRIPTION

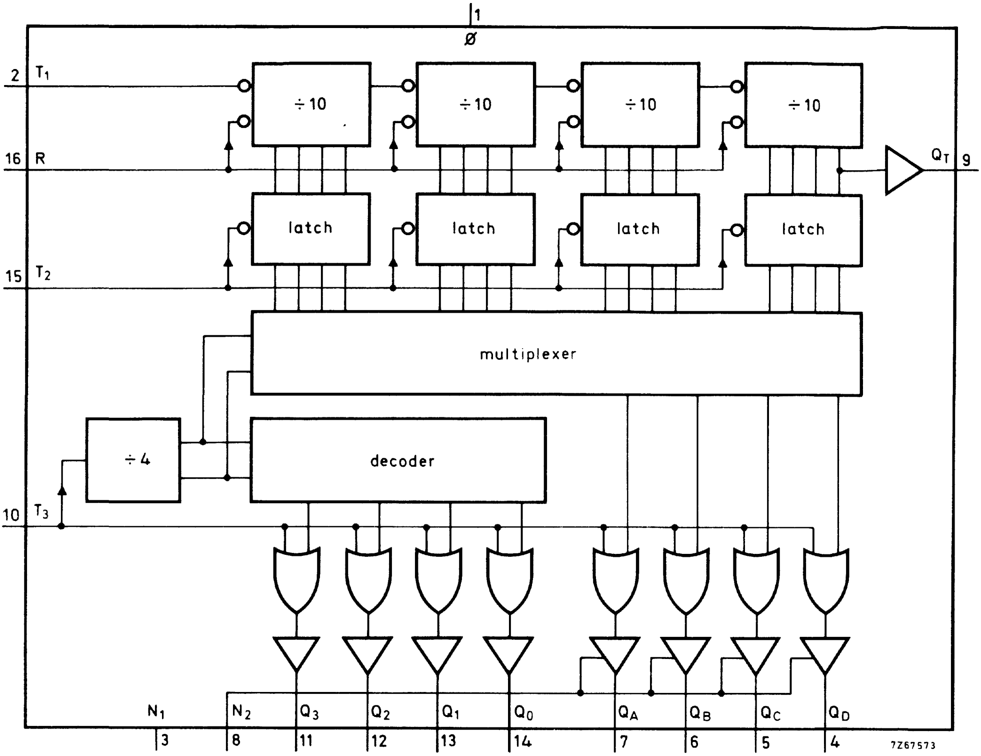
The FEJ271B consists of four cascaded decade counters, together with buffer registers and multiplexing circuitry for driving a digit-serial display unit.
The data outputs Q_A to Q_D show the contents of one of the four buffer registers in BCD code, and are designed to drive a TTL numerical indicator tube (N.I.T.) driver directly (e.g. the FJL101/7441A).

The scanning frequency is determined by input T_3 and can be matched to the requirements of a specific output system.

The outputs Q_0 to Q_3 give a continuous indication of which decade is connected to the data outputs; they are designed to drive the anode selection switch of a numerical indicator tube.

In order to increase the count capability beyond 4 decades, additional FEJ271B circuits can be connected in cascade. For this purpose the circuit is equipped with a carry output which can be connected to T_1 (count) input of the next FEJ271B in the cascade.
The input T_3 also acts as a chip select input, causing the outputs Q_0 to Q_3 to become HIGH, and allowing the data outputs Q_A to Q_D to be wire-OR-ed with the data outputs of other circuits.

LOGIC DIAGRAM



PINNING

1. ϕ : ground
2. T_1 : count input
3. N_1 : supply voltage
4. Q_D : data output D
5. Q_C : data output C
6. Q_B : data output B
7. Q_A : data output A
8. N_2 : supply voltage (V_{logic})
9. Q_T : carry output
10. T_3 : scan control
11. Q_3 : scan output
12. Q_2 : scan output
13. Q_1 : scan output
14. Q_0 : scan output
15. T_2 : transfer input
16. R : reset input

FUNCTIONAL DESCRIPTION

T_1 Count input

The counter changes state at the HIGH to LOW transition of the count pulse.

R Reset input

When R is LOW, all decades are reset to the "0" position, count input inhibited.

T_2 Transfer pulse input

When T_2 is LOW, the buffer registers will follow the decade counters.
When T_2 is HIGH, the outputs of the buffer registers remain unchanged.

T_3 Scan counter input/chip select input.

This input drives the scan counter, which triggers at the positive going edge of a T_3 pulse. By stepping the scan counter, the contents of the four buffer registers are subsequently passed to the data outputs.
Moreover, when T_3 is HIGH, all data and scan outputs become HIGH, thus allowing for co-operation of more FEJ271B circuits.

Q_A to Q_D Data outputs

These are current-sink type outputs with resistive pull-up. They show the contents of the buffer register selected by the scan counter in positive BCD code.
Q_A represents the least significant bit, Q_D the most significant.
The open circuit HIGH output voltage is zero, the open circuit LOW output voltage is V_{N2}.
The data outputs can directly drive a DTL/TTL decoder/N.I.T. driver and can be wire-OR-ed with the data output of other FEJ271B circuits.

Q_0 to Q_3 Scan outputs

These outputs show at each moment which buffer register is connected to the data outputs, in a 1 out of 4 code (one output LOW, the others HIGH).
Q_0 represents the least significant decade, Q_3 the most most significant.
They are open drain current source type outputs.
Scanning sequence: $Q_3 \rightarrow Q_2 \rightarrow Q_0 \rightarrow Q_1$

Q_T Carry output

This output is able to drive the T_1 input of another FEJ271B.
The output is HIGH when the most significant decade is in position 8 or higher, and LOW in all other cases.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltage of all pins with respect to pin 1 (ground)	V	+0,3 to −27	V
Data output current A (pin 7)	I_{QA}	+5 to −0,1	mA
Data output currents B, C, and D (pins 6, 5 and 4)	I_{QB}, I_{QC}, I_{QD}	+2,5 to −0,1	mA
Scan output currents (pins 14, 13, 12 and 11)	I_{Q0}, I_{Q1}, I_{Q2}, I_{Q3}	0 to −5	mA
Power dissipation in output stages	P_Q	max. 130	mW
Operating ambient temperature	T_{amb}	0 to +75	^oC
Storage temperature	T_{stg}	−65 to +125	^oC

CHARACTERISTICS at V_{N1} = −24 ± 1,5 V; V_{N2} = −4,75 to −5,25 V; T_{amb} = 0 to +75 ^oC

	Symbol		Conditions and references
Electrical data			
Input voltage HIGH pins 2, 10, 15 and 16	V_{IH}	> −1,5 V	
Input voltage LOW pins 2, 10, 16 pin 15	 V_{IL} V_{IL}	 < −9,0 V < −14 V	
Input leakage current	$-I_I$	< 10 μA	V_I = −10 V
Input capacitance	C_I	< 10 pF	
Scan output currents stage selected	 $-I_Q$	 < 20 μA	 open circuit drain I_{out} (off) at −20 V
stage not selected	$-I_Q$	> 1 mA	open drain conducting $I_{out\ (on)}$ at −1 V
Data output voltage LOW pins 4, 5, 6 and 7	V_{QL}	< 0,4 V	with respect to pin 8 at I_{QLmin}
Data output current LOW pin 7 pins 4, 5 and 6	 I_{QL} I_{QL}	 > 3,2 mA > 1,6 mA	 $V_{QL} = V_{N2}$ +0,4 V $V_{QL} = V_{N2}$ +0,4 V
Data output voltage HIGH pins 4, 5, 6 and 7	V_{QH}	> −2,3 V	at $-I_{QHmax}$
Data output current HIGH pin 7 pins 4, 5 and 6	 $-I_{QH}$ $-I_{QH}$	 < 80 μA < 40 μA	 at V_{QH} = −2,3 V
Data output leakage currents	$-I_Q$ I_Q	< 6 μA < 6 μA	at −5,25 V; T_3 = HIGH at 0 V; T_3 = HIGH

CHARACTERISTICS (continued)

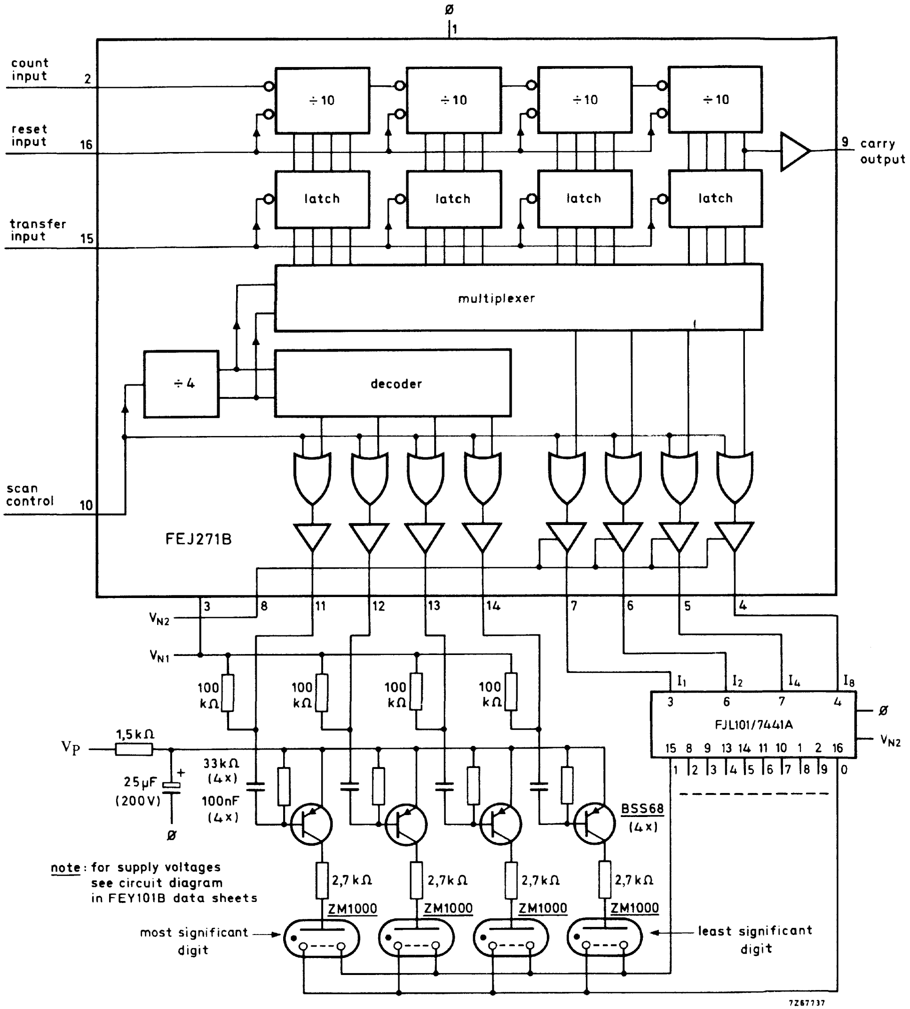
	Symbol		Conditions and references
Electrical data (continued)			
Carry output voltage HIGH	V_{QH}	> −1,5 V	at $-I_{QH}$ = 150 μA
Carry output voltage LOW	V_{QL}	< −10 V	I_{QL} = 10 μA
Supply data			
Supply currents	$-I_{N1}$	typ. 6,5 mA < 10 mA	
	$-I_{N2}$	see note	
Dynamic data			
Count input			
pulse duration	t_{T1}	> 0,25 μs	at 50% level
rise time	t_r	< 1 ms	10% to 90%
fall time	t_f	< 1 ms	10% to 90%
Reset input			
pulse duration	t_R	> 2 μs	at 50% level
rise time	t_r	< 1 ms	10% to 90%
fall time	t_f	< 1 ms	10% to 90%
Transfer input			
pulse duration	t_{T2}	> 2 μs	at 50% level
Scan control input			
pulse duration	t_{T3}	> 2 μs	at 50% level
Counting rate	f	0 to 1 MHz	
Scan clock input frequency	f	0 to 150 kHz	

Note

$-I_{N2}$ is sum of data output currents

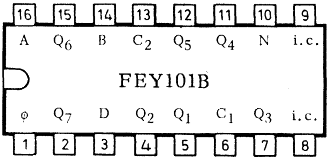
APPLICATION INFORMATION

A complete quadruple decade counter including display



The FE family is a series of monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

ANALOGUE/DIGITAL CONVERTER LOGIC



QUICK REFERENCE DATA				
Supply voltage	V_N		$-24 \pm 1,5$	V
Operating ambient temperature	T_{amb}		0 to +75	^oC
Measuring range			± 2000	div.
Sampling time			0, 2 to 4	s
Automatic polarity detection				
Power consumption	P_{tot}	typ.	130	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section)

GENERAL DESCRIPTION

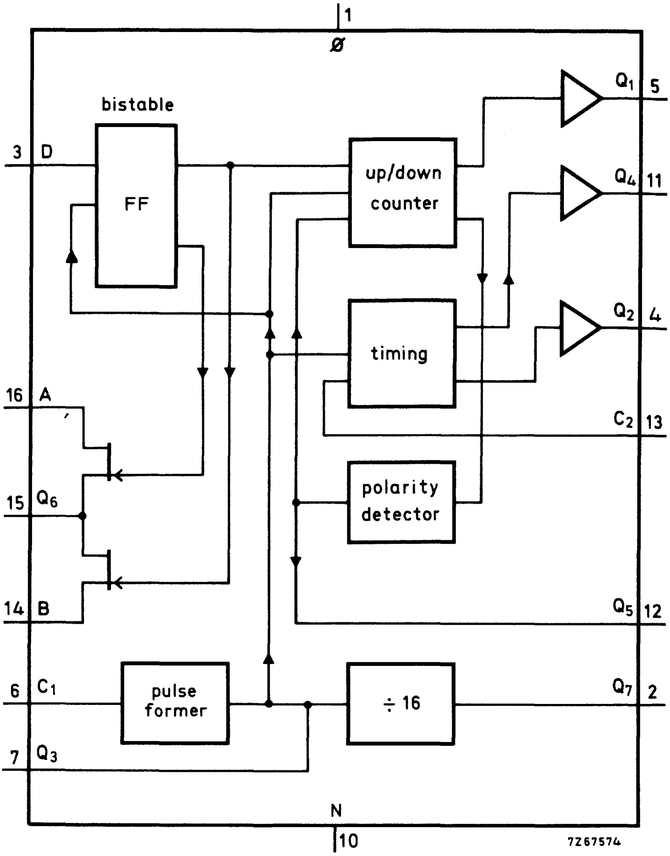
The FEY101B contains the logic parts of an integrated A/D type converter, designed for use in economic digital voltmeter systems.
It is intended to be used in combination with the FEJ271B (quadruple decade counter/register), an operational amplifier, a decoder/driver and some discrete components (see application information on pages 7, 8 and 9).
The output of the FEY101B is a serial type. The number of output pulses during a measuring period (between two transfer/reset pulses) is linearly proportional to the voltage measured.
The relationship between the number of output pulses (n), and the input voltage (V_i) is as follows:

$$n = |V_i| \cdot \frac{2046}{V_{ref}}$$

If V_{ref} is chosen as 2046 mV or 204, 6 mV, each output pulse then represents 1, 0 mV or 0, 1 mV respectively.

The circuit also gives an indication of the polarity of V_i.

LOGIC DIAGRAM



PINNING

1. ϕ : ground
2. Q_7: scan output
3. D : signal input
4. Q_2: transfer output
5. Q_1: pulse output
6. C_1: oscillator feedback input
7. Q_3: clock pulse output
8. i.c.
9. i.c.
10. N : supply voltage
11. Q_4 : reset output
12. Q_5 : polarity output
13. C_2 : synchronization input
14. B : $-V_{ref}$
15. Q_6 : chopper output
16. A : $+V_{ref}$

FUNCTIONAL DESCRIPTION

D — Signal input

To be connected with output of an operational amplifier.
HIGH: Q_6 connected to A; up/down counter counts up.
LOW : Q_6 connected to B ; up/down counter counts down.

Q_6 — Chopper output

When D is HIGH, this output is connected with A.
When D is LOW , this output is connected with B.

A and B — Reference inputs

Input A has to be connected with the positive reference voltage of the system and input B has to be connected with the negative reference voltage of the system.

Q_7 — Scan output

This output delivers a pulse for the scan input T_3 of the FEJ271B.
Its level is LOW during 15 clock periods and HIGH during one.

Q_1 — Pulse output

This output delivers a number of pulses during a measuring interval directly proportional to the input voltage and can be used for driving the pulse input T_1 of the FEJ271B.

Q_4 — Reset output

This output is HIGH during the measuring interval.
A LOW going pulse indicates the beginning of a measuring cyclus.
This LOW signal has the same duration as the HIGH signal of the clock-generator and is used for driving the reset input R of the FEJ271B.
During synchronization (see also C_2) more reset pulses will come.
The last of these pulses indicates the beginning of the real measuring interval of 4092 clock-periods.

Q_2 — Transfer output

Normally from HIGH to LOW going pulse, which indicates the end of a measuring cyclus.
Between the end of the real measuring interval and the end of the whole cyclus are a few clock periods (max. 16) for clearing the internal up/down counter.
This pulse can be used for driving the transfer input T_2 of the FEJ271B.

Q_5 — Polarity output

This output drives the polarity indication.
HIGH: input voltage of the system is negative.
LOW : input voltage of the system is positive.

FUNCTIONAL DESCRIPTION (continued)

C_1 Oscillator feedback input

This input has to be connected via a capacitor of 180 pF with Q_3 to obtain a clock frequency of typical 8 kHz.

C_2 Synchronization input

When this input is LOW the system does not start a new measuring interval untill there is a positive going slope on input D.
This results in a flickerless display of the last digit.
Blocking the whole system when applying too high input voltages can be avoided by limiting the time when C_2 is LOW to approximately 1 ms.

Q_3 See C_1.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage of all pins with respect to pin 1 (ground)	V	+0, 3 to −27	V
Power dissipation	P_{tot}	max. 275	mW
Operating ambient temperature	T_{amb}	0 to +75	°C
Storage temperature	T_{stg}	−65 to +125	°C

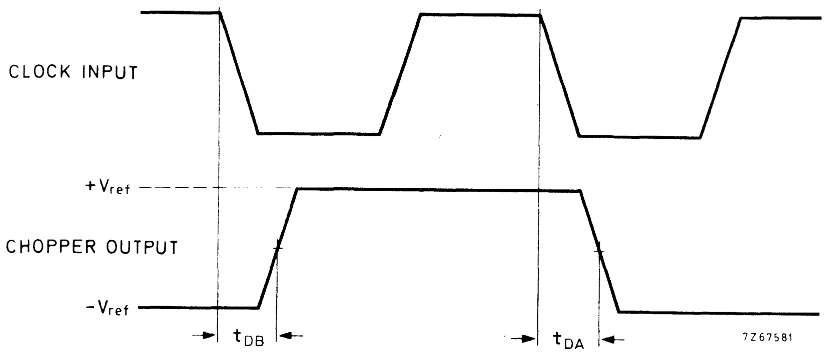
CHARACTERISTICS at V_N = −24 ± 1, 5 V; T_{amb} = 0 to +75 °C (unless otherwise specified)

	Symbol		Conditions and references
Input data			
Signal input (D)			
Input voltage HIGH	V_{IH}	> −2 V	
Input voltage LOW	V_{IL}	< −10 V	
Input resistance	R_I	> 60 kΩ < 200 kΩ	with respect to ground
Synchronization (C_2)			
Input voltage HIGH	V_{IH}	> −2 V	
Input voltage LOW	V_{IL}	< −8 V	
Input leakage current	I_I	< 1 μA	V_I = −8 V
Reference inputs (A;B)			
Reference voltages; pin 14 pin 16	$-V_{ref} = V_B$ $+V_{ref} = V_A$	0 to −9 V	with respect to ground
"ON" resistance unbalance	ΔR_{on}	< 400 Ω	$\lvert V_A - V_B \rvert$ = 4 V
Input leakage current	$\lvert I_I \rvert$	< 1 μA < 100 nA [1]	with respect to ground at − 9 V
Input leakage current	$\lvert I_I \rvert$	< 1 μA < 100 nA [1]	with respect to pin 15 at −9 V

[1]) At T_{amb} = 25 °C

CHARACTERISTICS (continued)

	Symbol		Conditions and references
Output data			
Scan, reset and pulse outputs (Q_7, Q_4 and Q_1)			
Output voltage HIGH	V_{QH}	> −1,5 V	$-I_{QH}$ = 100 μA
Output voltage LOW	V_{QL}	< −9 V	I_{QL} = 10 μA
Transfer output (Q_2)			
Output voltage HIGH	V_{QH}	> −1,5 V	$-I_{QH}$ = 100 μA
Output voltage LOW	V_{QL}	< −14 V	I_{QL} = 1 mA
Polarity output (Q_5)			
Output current HIGH	$-I_{QH}$	> 1 mA	V_{QH} = −4 V
Output current LOW	I_{QL}	typ. 0,1 μA < 8 μA	V_{QL} = −8 V
Supply data			
Supply current	$-I_N$	typ. 5,5 mA < 10 mA	
Dynamic data			
Switching speed balance	$\|t_{DA}-t_{DB}\|$	< 650 ns	see waveform below
Oscillator			
Frequency range by external adjustment	f	1 to 20 kHz	capacitor between pins 6-7
Capacitor value for f = 8 kHz	C	typ. 180 pF	

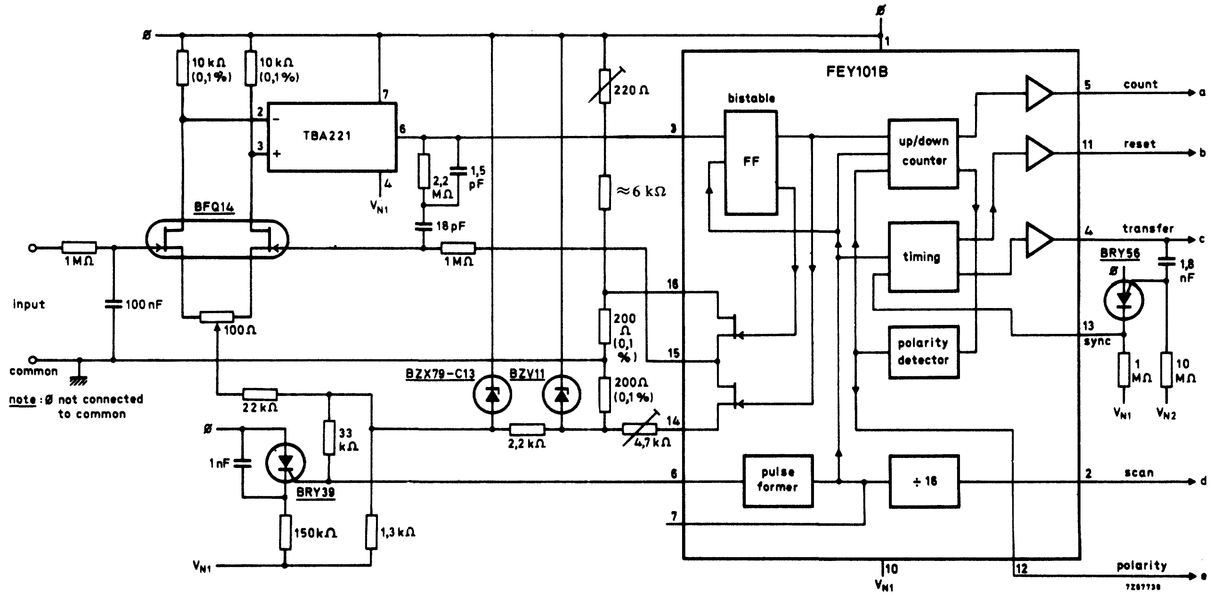


TYPICAL PERFORMANCE

The FEJ271B and FEY101B used in a digital voltmeter (see pages 7, 8 and 9)

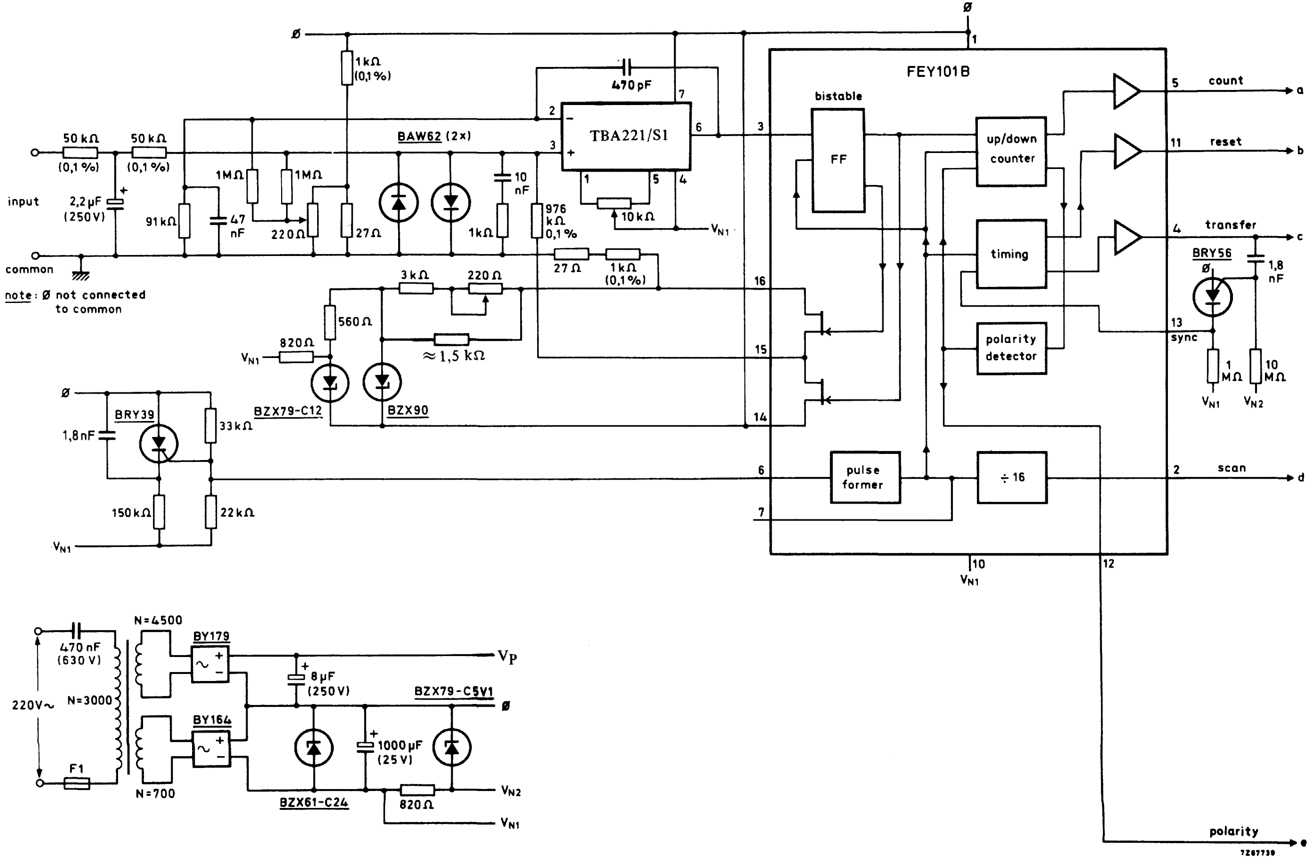
	without input FET's	with input FET's	
Input sensitivity	1	–	MΩ/V
Input impedance	–	> 100	MΩ
Sampling time	0,8	0,5	s
Settling time	1	1	s
Range (automatic polarity)	± 100	± 100	mV
Over-range	100	100	%
Accuracy (of full scale)	0,4	0,15	%
Resolution	100	100	μV

APPLICATION INFORMATION

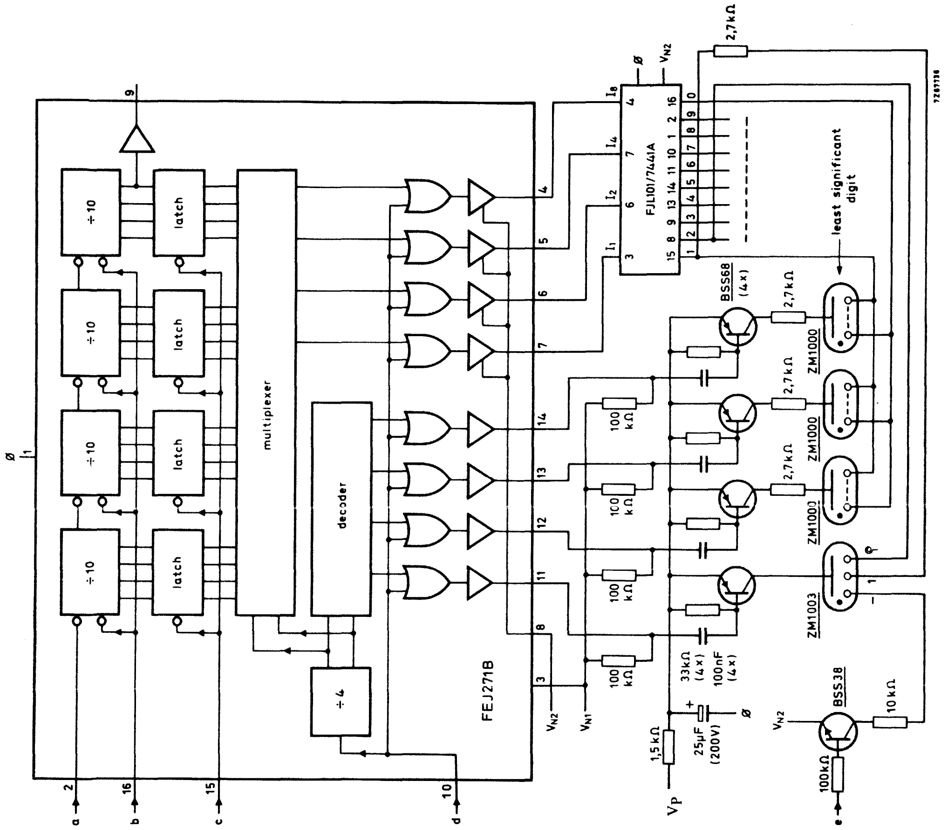


DVM with input FET's to provide extremely high input impedance
(counter part of circuit is continued on page 9)

APPLICATION INFORMATION (continued)



DVM with 1 MΩ/V input sensitivity
(counter part of circuit is continued on page 9)


÷10
latch
multiplexer
decoder
÷4
FEJ271B
FJL101/7441A
BSS68
(4x)
2,7kΩ
ZM1000
ZM1003
least significant digit
100 kΩ
33kΩ (4x)
100nF (4x)
25μF (200V)
1,5kΩ
BSS38
10kΩ
100kΩ
V_P
V_{N1}
V_{N2}

INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availability.

Type No.	Section	Type No.	Section	Type No.	Section
FCH101	DTL	FDN216B	MOS	GXB10131	CML
FCH111	DTL	FDN506	MOS	GXB10160	CML
FCH121	DTL	FDN536A	MOS	GXB10161	CML
FCH131	DTL	FDR116Z	MOS	GXB10162	CML
FCH141	DTL	FDR116Z1	MOS	GXB10164	CML
FCH151	DTL	FDR116Z2	MOS		
FCH161	DTL	FDR126Z	MOS		
FCH171	DTL	FDR126Z1	MOS		
FCH181	DTL	FDR131Z	MOS		
FCH191	DTL	FDR131Z1	MOS		
FCH201	DTL	FDR131Z2	MOS		
FCH211	DTL	FDR146Z	MOS		
FCH221	DTL	FDR146BZ	MOS		
FCH231	DTL	FDR146Z1	MOS		
FCH281	DTL	FDR146BZ1	MOS		
FCH291	DTL	FDR146Z2	MOS		
FCH301	DTL	FDR146BZ2	MOS		
FCH311	DTL	FDR151Z	MOS		
FCH321	DTL	FDR151BZ	MOS		
FCJ101	DTL	FEJ271B	MOS		
FCJ111	DTL	FEY101B	MOS		
FCJ121	DTL	GXB10101	CML		
FCJ131	DTL	GXB10102	CML		
FCJ141	DTL	GXB10105	CML		
FCJ191	DTL	GXB10106	CML		
FCJ201	DTL	GXB10107	CML		
FCJ211	DTL	GXB10109	CML		
FCJ221	DTL	GXB10110	CML		
FCK111	DTL	GXB10111	CML		
FCL101	DTL	GXB10115	CML		
FCY101	DTL	GXB10117	CML		
FDN166A	MOS	GXB10118	CML		
FDN196A	MOS	GXB10119	CML		
FDN196B	MOS	GXB10121	CML		
FDN216A	MOS	GXB10130	CML		

DTL = FC family
MOS = FD/FE family
TTL = FJ/GJ family
CML = GX family

MAINTENANCE TYPE LIST

The integrated circuits listed below have become maintenance types, therefore abridged information is included in this handbook

FDN166A
FDN196A
FDN196B
FDN216A
FDN216B
FDN506
FDN536A

General	
DTL	FC family
CML	GX family
MOS	FD family
MOS	FE family